The influence of TiW and Ti-TiN interface layers on power transistor parameters

Miroslav Sumega [1], Vladimír Áč [2]
[1] ON Semiconductor Piešťany a.s., Vrbovská cesta 102, 92101 Piešťany
[2] Alexander Dubček University of Trenčín, Študentská 2, 91150 Trenčín
E-mail : vac@tnuni.sk

Abstract:
The power MOS transistors were tested with different diffusion barrier type used in metallization contact stack. The contact structure in integrated circuit (IC) needs to have good ohmic properties with low contact resistance and it needs to be thermodynamically stable to prevent contact degradation. Because high current operation the power transistors in IC should be most sensitive parts for barrier stability testing. The PtSi-TiW-AlCu metallization technology will by compared with PtSi-Ti-TiN-AlCu metallization. Generally, the TiW diffusion barrier has lower thermodynamic stability with AlCu metallization compare to TiN. Therefore a Ti-TiN barrier implementation could be attractive for manufacturing using TiW barrier technology. It will be interesting to test the R_{ON} (transistor resistance in switch ON state), gate threshold voltage and leakage current parameters on power MOS transistors because the barrier changes. The barrier and aluminium-copper interface will be compared on the SEM cross-sections samples.

INTRODUCTION

The power metal oxide semiconductor field effect transistor (MOSFET) is based on the original MOS transistor scheme with poly-silicon gate; in this work tested. The basic difference is in transistor dimensions. The transistor dimensions are designed to be able work with higher voltage and current without to run out of maximum temperature limits.

The power MOS transistor was developed to overcome bipolar power transistor limitations in microelectronics applications. The switch speed limitation. On other hand, the MOS transistors limitation in comparison to bipolar transistor is lower breakdown voltage level for the same transistor dimensions. In this work, we will test the p-type power MOS transistor and the n-type power MOS transistor with different diffusion barrier used in metallization stack [1]. The contact structure is a part of the transistors also and could change the device functionality. Important contact properties are a low contact resistance, because the current losses or signal time delays and the thermal stability with the silicon. The direct contact to silicon is created with silicide layer. In this work, the PtSi silicide is used. Between the silicide layer and interconnect metallization (AlCu with 0.5% Cu) layer, TiW and Ti-TiN diffusion barrier layers were tested. The barrier is necessary because Si solubility in AlCu layer. This is starting mechanism for junction spiking. Titanium tungsten was among the first material to be employed as a diffusion barrier a typically used with PtSi layer [2]. Titanium nitride is an attractive material as a contact diffusion barrier in silicon manufacturing because it behaves as an impermeable barrier to silicon and because the activation energy for the diffusion of other impurities is high. The TiN specific contact resistivity to Si is somewhat higher than that of Ti or PtSi, and as result, it is ordinary not used to make direct contact to Si. Instead, it was most commonly been used in contact structure consisting of Al-TiN-Ti or $TiSi_2$-Si [3-4].

MOSFET TRANSISTOR

The n-type (p-type) MOS transistor consists of a source and a drain, two highly conducting n-type (p-type) semiconductor regions, which are created into the p-type (n-type) substrate region. A poly-crystalline gate covers the region between source and drain. The gate is separated from the semiconductor by the gate silicon oxide layer. The substrate is contacted to the source electrode. The voltage applied to the gate controls the flow of electrons (holes) from the source to the drain. A positive (negative) voltage applied to the gate attracts electrons (holes) to the interface between the gate dielectric and the semiconductor. These electrons (holes) form a conducting channel. The result is that the applied gate voltage controls the current between the drain and source.

Threshold voltage, V_{th} is defined as a minimum gate electrode bias required to strongly inverting the surface under the poly-silicon and forms a conducting channel between the source and the drain regions.

The R_{ON} resistance of MOS transistors (transistor resistance if transistor is switch ON state) is built up of several components.

$$R_{ON}=R_{source}+R_{ch}+R_{drain}+R_{wcml},$$

where R_{source} is a source diffusion resistance, R_{ch} is a channel resistance, R_{drain} is a drain diffusion

resistance and R_{wcml} is a sum of bond wire resistance, contact resistance between the source and drain metallization and the silicon metallization. These are normally negligible in high voltage applications but can become significant in low voltage applications.
The leakage current is defined as maximum allowed current through drain – substrate diode reverse biased. The channel is closed (accumulated), the source and substrate are connected to the ground and the drain to the voltage bias.

EXPERIMENTAL

The measurement was made on ON Semiconductor Piestany product NCP1582. The power transistors gate oxide thickness was 35nm. The gate dimensions were 2.2µm x 215µm (length x width). The structure is built as 160 gates electrodes net with 4µm gap between them, where is implanted drain-source region (with B or As). The TiW barrier was deposited on the varian#3290 equipment from single target (90%W, 10%Ti). The Ti-TiN barrier was deposited on the MRC Eclipse Mark4 equipment; from single Ti target in Ar-N2 ambient. The electrical characteristics were measured on production wafers; five test structures on one 6 inch wafer. In presented charts, normal distribution functions calculated from mean value and standard deviation of the measured samples are compared. The contact structure with the TiW, the TiW insitu deposited with the AlCu, the TiN and the Ti-TiN barriers were tested.

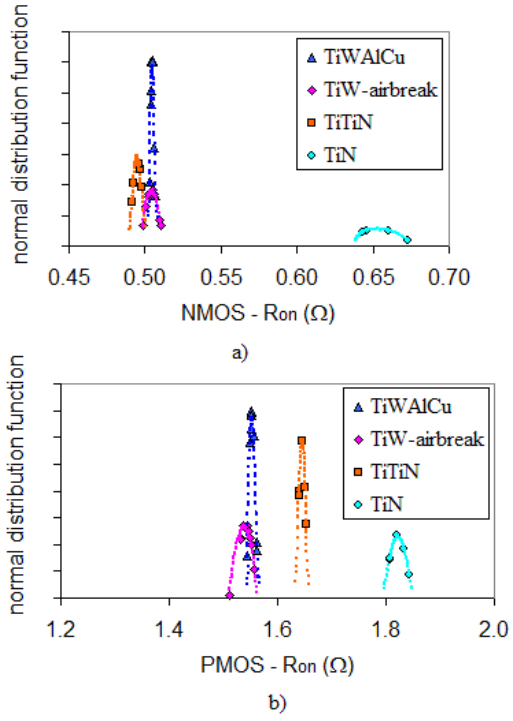

Fig. 1: Transistor R_{ON} vs. barrier type; a) for NMOS transistor; b) for PMOS transistor.

The R_{ON} parameter mainly represents the contact resistance change with different barrier use in metallization stack. The normal distribution characteristics for each barrier type are shown in figure 1. The difference by the work function of the barrier material for Ti-TiN and TiW diffusion barrier is seen. For NMOS, the R_{ON} is lower with use of Ti-TiN barrier and it is backwards for PMOS transistor. The R_{ON} is the highest for both transistor types with the use of TiN barrier.

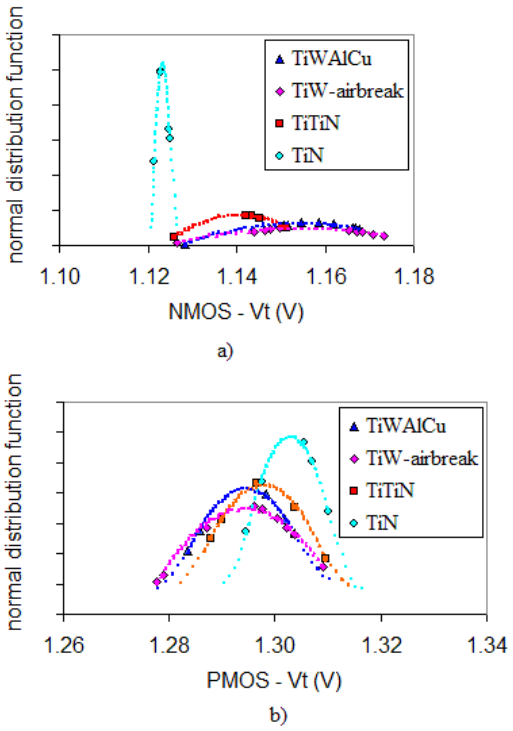

Fig. 2: Transistor *Vt* vs. barrier type; a) for NMOS transistor; b) for PMOS transistor.

It was observed that the threshold voltage is influenced with the diffusion barrier change (see Fig. 2). The shifts are made with the barrier work function change. It is visible that the air-break between barrier and metallization has not significant influence on R_{ON} and also on V_t characteristics.
The barrier thermodynamic stability was tested with leakage current between transistor's drain and substrate. Higher leakage current values are possible to seen from Fig. 3. for TiW barrier deposited insitu with AlCu layer on NMOS transistor only.
The barrier degradation was confirmed on the cross-section samples. The contact structure to the drain region was compared (see Fig. 4). In the pictures, the cross-section through contact structure to doped silicon region is shown.
It is visible that the interface between the TiW barrier and aluminium-copper in situ deposited is rougher compare to the others (see Fig. 4b). There are visible spikes through the TiW barrier. The barrier started to decompose on the surface. On other hand, the TiW barrier surface deposited with air-break between the

barrier and aluminium-copper is ideally smooth (see Fig. 4c).

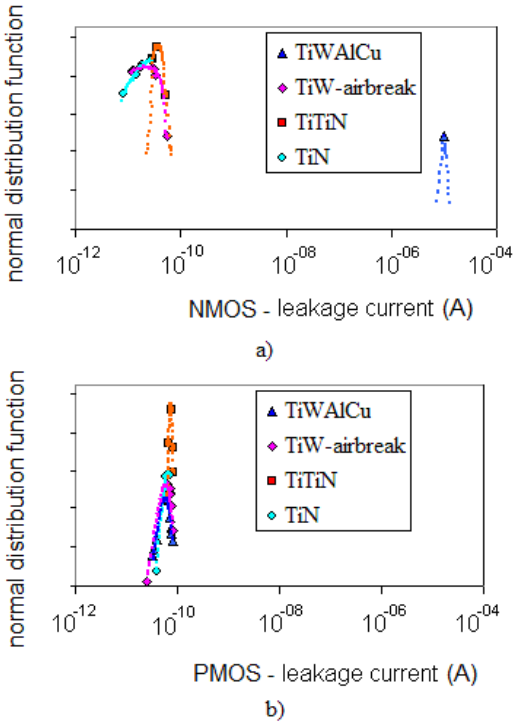

Fig. 3: Transistor *Ileakage* current vs. barrier type; a) for NMOS transistor; b) for PMOS transistor.

The Ti-TiN barrier surface roughness is not the same compare to the TiW barrier deposited with air-break. The roughness onto the Ti-TiN barrier surface suggests that the titanium with the aluminium form a titanium-aluminid (see Fig. 4a). This effect was confirmed with the sheet resistance measurement [5]. The transistor leakage current measurement confirms that through the Ti-TiN barrier the aluminium-copper layer does not penetrate.

CONCLUSIONS

The power MOS transistor parameters were characterized with the barrier change. The electrical parameters depend on a barrier work function, on the specific contact resistance and on the thermal stability between barrier and aluminium layers.

With the TiW barrier limitation, the Ti-TiN barrier thermal stability was shown. The barrier limitation was confirmed with the SEM cross-section pictures. The AlCu penetrates easier through the TiW barrier without air break and degraded the contact. The AlCu atoms (p-type) doped the n-type region. This mechanism degraded the n-type drain region [6].

Based on the R_{ON} characteristics results, the TiN barrier could be used only with Ti under layer which was tested also. It is given by the reactive sputtering in the N_2 ambient. The titanium nitride on PtSi surface increases the transistor contact resistance.

From reliability test point of view this characterizations suggests, the Ti-TiN barrier could be applicable for manufacturing.

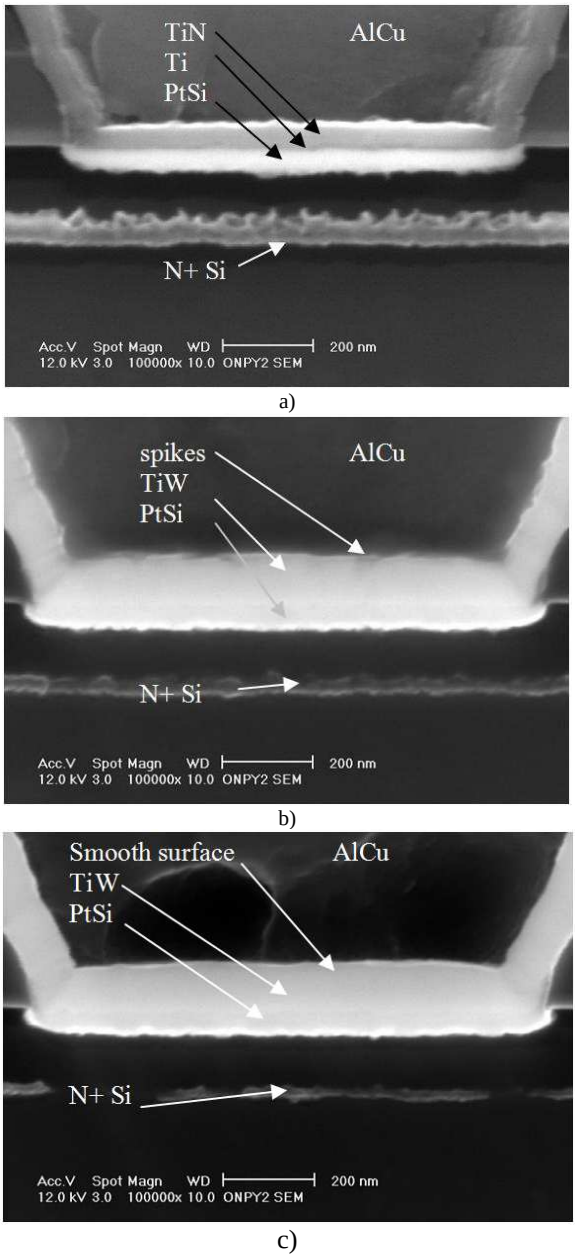

Fig. 4: Cross-section through contact to drain region.; a) Ti-TiN barrier; b) insitu TiW barrier; c) air-break TiW barrier.

ACKNOWLEDGEMENTS

This work was supported by ON Semiconductor Piestany and by the Slovak Ministry of Education Scientific Grant Agency VEGA under the project No. 1/4134/07.

REFERENCES

[1] V. Barkhordarian, "Power MOSFET Basics, International Rectifier", www.irf.com/technical-info/appnotes/mosfet.pdf

[2] T. Castan, J.-L Peyre. K. Beschorner, "High-throughput W/Ti barrier sequential deposition", Solid State Technology, Vol. 41, June 1998, pp.127-8, 130, 132

[3] L. Ting, Q.-Z. Hong, "Effect of heat treatments on electromigration performance for TiN-AlCu-TiN interconnect", Proc. of the SPIE - The International Society for Optical Engineering, Vol. 69, 1994, pp. 2134-6

[4] S. H. Kim, S. S. Yim, D. J. Lee, K. S. Kim, H. M. Kim, K. B. Kim, H. Sohn, "Diffusion Barriers Between Al and Cu for the Cu Interconnect of Memory Devices", Electrochem. Solid-State Lett., Vol. 11, Issue 5, 2008, pp. H127-H130

[5] L. Ting, Q.-Z. Hong, "Effect of heat treatments on electromigration performance for TiN-AlCu-TiN interconnect", Proc. of the SPIE - The International Society for Optical Engineering Vol. 69, 1994, pp. 2134-6

[6] G. Galvagno , A.L. Ferla, F.A. Via., V. Rainer , A. Gasparotto, A. Carnera, E. Rimini: "Hole mobility in aluminium implanted silicon", Semicond. Sci. Technol., Vol. 12, 1997, pp. 1433-1437