First Order Current-Mode Universal Building Block

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Abstract:

This paper deals with design of second generation current conveyor and transconductance amplifier for the 1st order current-mode universal building block. The universal building block is able to provide transfer of high-pass and low-pass in one circuit. With the multi-output CCII and OTA, it is possible to create various transfer function.

The current conveyor is designed to have very low input impedance and very high output impedance. For this purpose auxiliary feedback was used for port X and original arrangement of output current mirrors decreasing supply power. Transconductance amplifier is based on simple differential pair in the input stage.

INTRODUCTION

In [7] we have early presented an idea of the 1st-order universal current-mode building block suitable for a low-pass, high-pass and all-pass filter realizations. The purpose of this paper is to show a CMOS implementation of such a block and to present the real properties of the designed circuit. The general block diagram of the universal block is shown in Fig. 1. As evident, a current follower (CF) and a transconductance amplifier (OTA) are the basic sub-blocks.

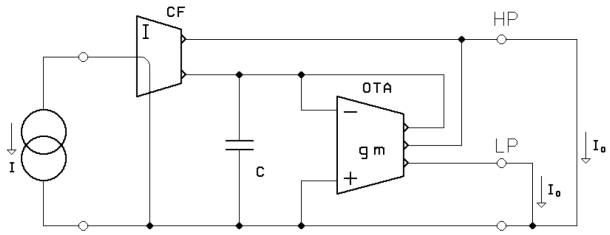

Fig. 1: First order current-mode building block [7]

The final solution is based on a Double-Output Current Conveyor (DOCCII+) serving as a current follower and a multiple-output transconductance amplifier. The specified block diagram is introduced in Fig. 2. As can be easily derived, the main transfers

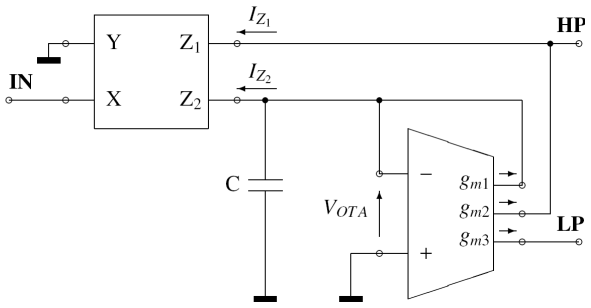

Fig. 2: First order current-mode building block – final form

corresponding to the low-pass and high-pass filters are expressed by Eqs. (1) and (2) in the form

$$H(s)_{LP} = \frac{\beta_2 g_{m3}}{sC + g_{m1}}; \qquad (1)$$

$$H(s)_{HP} = \frac{\beta_2 g_{m2}}{sC + g_{m1}} - \beta_1 . \qquad (2)$$

Note that the setting of $\beta_1 = \beta_2 = \beta$ and $g_{m1} = g_{m2} = g_m$ leads to the simplification of the previous equations (1), (2) to the form (3):

$$H(s)_{LP} = \frac{\beta}{1 + s\tau}; \; H(s)_{HP} = \beta \frac{s\tau}{1 - s\tau}, \qquad (3)$$

where $\tau = \frac{C}{g_m}$.

BUILDING BLOCK DESIGN

Now, let us an attention to the sub-blocks design. The additional requirements to their properties are as follows:

1. The positive second-generation current conveyor with double output (DOCCII+) has port Y grounded. Port X creates an input port of the block. That's why the input impedance needs to be as low possible.
2. The transconductance g_m of the transconductance amplifier (OTA) is given by possible values of integrated capacitor and frequencies in the range of tenths of MHz. According to this, g_m should be at least 100µS and OTA needs also a triple output with equal characteristics.

3. Current mirrors are the critical parts of both the partial blocks. In accordance to Ref. [9], the cascode current mirrors with external biasing were used. This provides high output impedance, high bandwidth and reasonable input voltage and minimum output voltage lower than common cascode mirror.

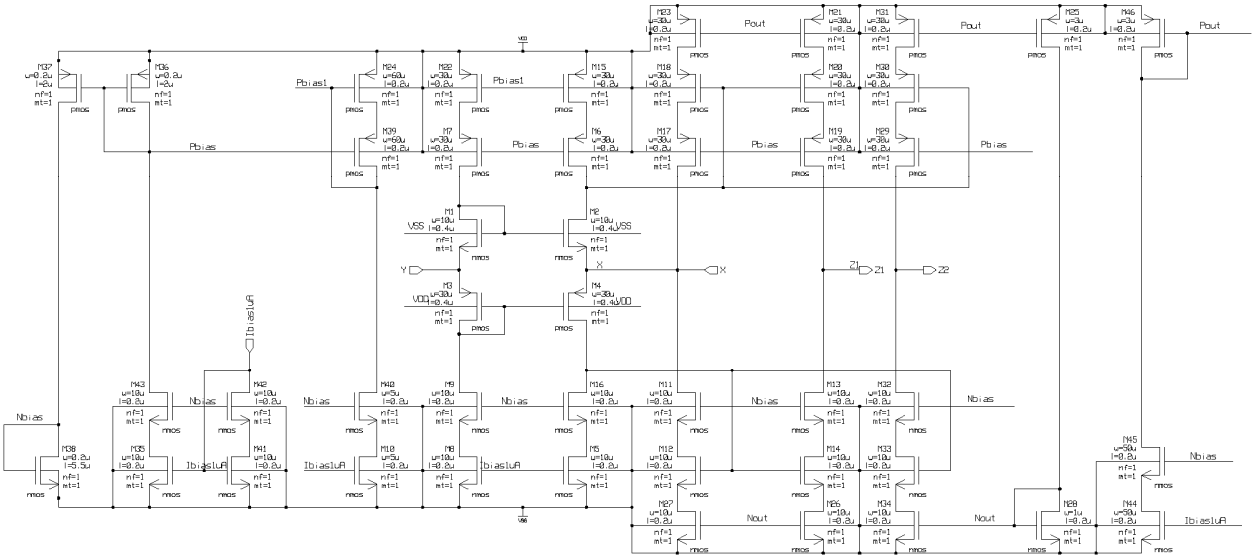

Fig. 3: Double Output Current Conveyor DOCCII+

Current Conveyor (CC)

The input stage of DOCCII+ is translinear loop in class AB. To create current input with low input impedance, the modification of translinear loop [3] was used. The input current now flows mainly through the added current mirrors and not through the translinear loop. This is why the operating point of the translinear loop does not alter with input current and provides good voltage transfer from the port Y to X. The feedback decreases input impedance on the current input X according to feedback loop gain.

This modification leads to very high current (1mA) flow through output mirrors and make proper function of them impossible because transistors runs out from saturation. It was necessary to set the current lower, but preserve low input impedance on port X.

The additional resistors were added in series with current mirrors as is commonly used for increasing output impedance. This arrangement decreases voltage on gates of transistors in output mirrors and does not change the signal path. The resistors are finally replaced by other transistors in connection known as active load. The output impedance is now greater and power consumption is reasonable. Output voltage range is quite decreased by voltage on two extra transistors but it is acceptable.

The double output of DOCCII+ is done by duplication of the output mirrors. Both outputs have equal characteristics and current transfer β can be easily changed for each output independently.

The final circuit diagram is shown in Fig. 3. Designed CC has current transfer β = 0,997 with offset I_{OFFSET} = - 66nA@I_{IN}=0 and input current range ±100µA. Power consumption with zero input signal is 1,4mW (350µA at 4V). Input impedance of port X and output impedances on both port Z1 and Z2 are in Table 1. Gain bandwidth given by 3dB decrease of current transfer is 512 MHz.

Tab. 1. Input and output impedances of designed DOCCII+ and TOOTA

Frequency	***DOCCII+***		***TOOTA***	
	input impedance	output impedance	input impedance	output impedance
0,1 MHz	47 Ω	52 MΩ	99 MΩ	147 MΩ
1 MHz	50 Ω	52 MΩ	24 MΩ	152 MΩ
10 MHz	172 Ω	50 MΩ	2.5 MΩ	161 MΩ
100 MHz	2015 Ω	40 MΩ	0.25 MΩ	161 MΩ

Transconductance amplifier (OTA)

Transconductance amplifier is designed to have transconductance g_m at about 100µS and triple output with identical characteristics with ability to change g_m independently. The low g_m allow to use quite high tail current (I_{SS} = 100µA) of differential pair to achieve linearity better than 1% for differential input voltages in range about ±160mV.

Final transconductance of the TOOTA is g_m = 192 µS with bandwidth 184 MHz. Input and output impedances are summarized in Table 1. Output impedance is simulated with differential input voltage V_{IN} = 100mV and output voltage 0 and 100mV.

The designed current-mode building block properties

The designed sub-blocks DOCCII+ and TOOTA were used for the 1st order current-mode building block simulation in accordance to the Fig. 2.

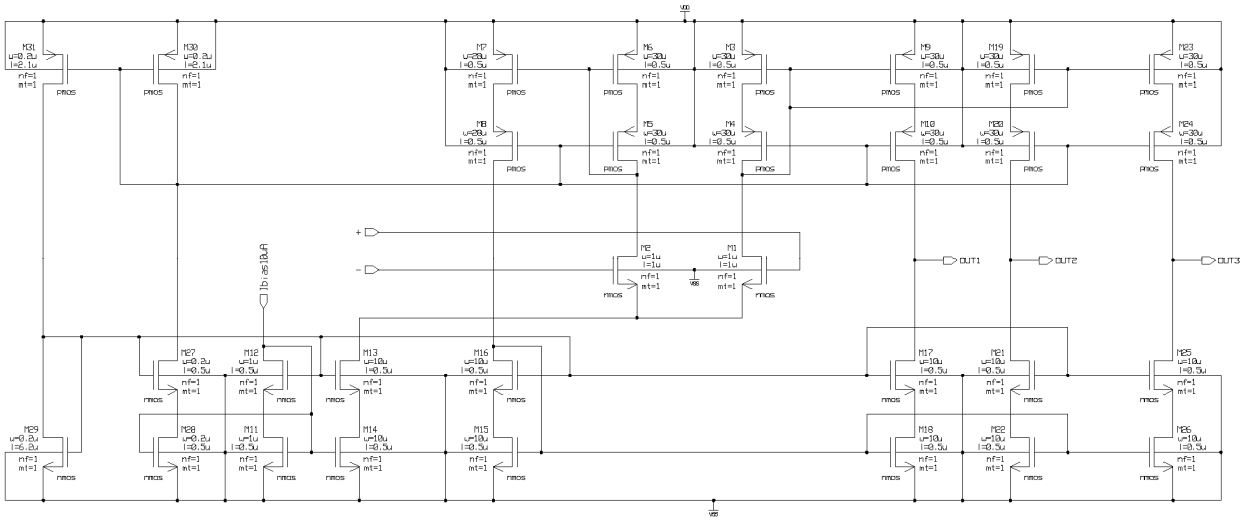

Fig. 4: Double Output Current Conveyor DOCCII+

For C = 2pF, β = 0,997 and g_m = 192 µS we get the LP pole output 15 MHz. Figure 5 shows a comparison of block assembled from the ideal blocks with provided parameters (curves "HP id" and "LP id") to the designed blocks (curves "HP" and "LP"). The differences in critical points are just a few tenths of dB. The lowest current transfer of output HP is -43dB, in the pass-band is about +1dB. Current transfer of output LP is -0,1dB in the pass-band.

CC possible improvement

The presented circuit of DOCCII+ is a subject of further research and is being redesigned to allow lower power supply voltage and to migrate to 1µm technology. For all current mirrors in circuit were used regulated cascode current mirrors [11]. Operation points of transistors were set to inversion coefficient IC between 0.1 and 1. This brings us high accuracy of current transfer β = 0,998 and extremely high output impedance. Power consumption decreases under 50µW at power supply voltage 1.2V for zero input signal. Input currents range is now ±5µA. Gain bandwidth falls down to 25 MHz.

CONCLUSION

Presented circuit is designed and simulated in CMOS technology. The characteristics show that it is possible to use the building block in current mode circuits for frequencies up to 180MHz. The main contribution of this paper is the design of current conveyor. The improvement of traditional circuit decreases input impedance and power consumption and increases output impedance together with wide bandwidth with maximum frequency at 512 MHz.

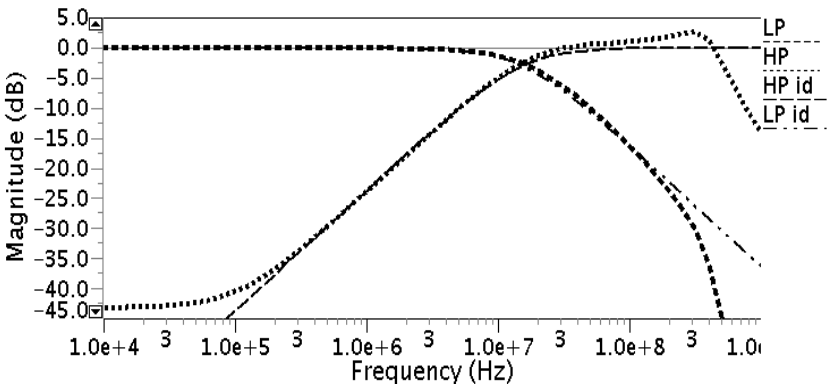

Fig. 5: The simulated frequency responses

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