New High Performance CMOS Fully Differential Current Conveyor

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***Abstract*— In this paper, a new CMOS high performance fully differential second-generation current conveyor (FDCCII) is presented. The proposed FDCCII provides good linearity, high output impedance at terminals Z+ and Z-, and excellent output–input current gain accuracy. What is more, it is operated at lower supply voltage of ± 1.25 V. As an application, a published current mode universal filter is realized with proposed FDCCIIs to demonstrate its versatility. The proposed FDCCII and its applications are simulated by using CMOS 0.35 µm technology.**

Index Terms— **Current conveyors, CMOS analog integrated circuits, Active filters.**

I. INTRODUCTION

An analog circuit design using the current mode approach has recently gained considerable attention, because of its inherent advantages such as wide bandwidth, high slew rate, low power consumption, and simple circuitry [1]. The second generation current conveyor (CCII) is one of the most versatile current mode building blocks. Since its introduction [2], several circuit realizations have been made for its implementation [3]-[8]. The CCII is a single-ended device; however, most modern high-performance analog integrated circuits incorporate fully differential signal paths. This is because fully-differential circuit configurations have been widely used in high-frequency analog signal applications such as switched capacitor filters [9] and mute-standard wireless receivers [10]. As compared to their single-ended counterparts, they have higher rejection capabilities to clock-feed-through, and to charge injection errors and power supply noises. They also have a larger output dynamic range, higher design flexibility, and reduced harmonic distortion. Moreover, most modern systems employ both analog and digital parts on the same chip. A fully differential architecture of the analog part becomes more essential as it provides immunity to digital noise.

In this study, a new implementation for FDCCII is proposed, based on an improved active-feedback cascode current mirror (IAFCCM) [11]. The output resistances at terminals Z+ and Z- of the proposed FDCCII are calculated and it provides high output resistances, compared with its published counterpart cascode FDCCII, theoretically [12, 13]. The circuit exhibits also excellent output–input gain accuracy both in voltage and current mode [14]. Besides, as an application, a current-mode universal filter chosen from the literature, by employing the proposed fully differential current conveyor (FDCCII) is simulated [15].

II. THE PROPOSED CIRCUITS

The FDCCII is basically a fully differential device as shown in Fig. 1. Using standard notation, the symbol of FDCCII shown in Fig. 1 and its i-v relationship is given by matrix equation in Eq. (1)

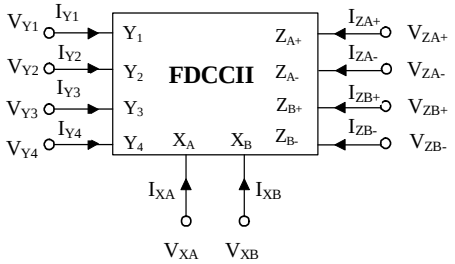

Figure 1. The Symbol of the FDCCII

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Y4} \\ V_{XA} \\ V_{XB} \\ I_{ZA\pm} \\ I_{ZB\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \pm 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \\ I_{XA} \\ I_{XB} \\ V_{ZA\pm} \\ V_{ZB\pm} \end{bmatrix} \quad (1)$$

The CMOS realization of the cascode FDCCII is shown in Fig. 2 [12]. It is possible to increase the output resistances and the accuracy of the current transformations of FDCCII by using the cascode current mirrors between terminals X and Y, X and Z+, and Y and Z as shown in Fig. 2. The Z– output resistance of the cascode FDCCII is given by Eq. (2).

$$R_{z-} \cong (r_{ds34} r_{ds33} g_{m34}) // (r_{ds35} r_{ds36} g_{m35}) \quad (2)$$

Where r_{ids} and g_{mi} denote the output resistance and small signal transconductance of the *i*th transistor, respectively.

To increase the output resistance of the proposed FDCCII the improved active-feedback cascode current mirrors (IAFCCM) are added to the circuit [11] by designing the output stages. The proposed high performance FDCCII is shown in Fig. 3. A major advantage of IAFCCM circuit is that

the output conductance and the feedback capacitance are 100 times lower than the standard current mirror circuit [11].

Although the number of transistors used in its implementation of new FDCCII are more than its counterpart the output resistance is much higher. The output resistance at terminal Z of new FDCCII shown in Fig. 3, is calculated as in Eq. (3)

$$R_{z-} \cong [g_{m3N1} g_{mKN1} r_{ds3N1} r_{ds2N1} (r_{dsKN1} // r_{dsCN1})] // [g_{m3P1} g_{mKP1} r_{ds3P1} r_{ds2P1} (r_{dsKP1} // r_{dsCP1})] \quad (3)$$

From Eq. (3) it can be seen easily that the output resistance of the proposed FDCCII is much higher than the published counterpart cascode FDCCII.

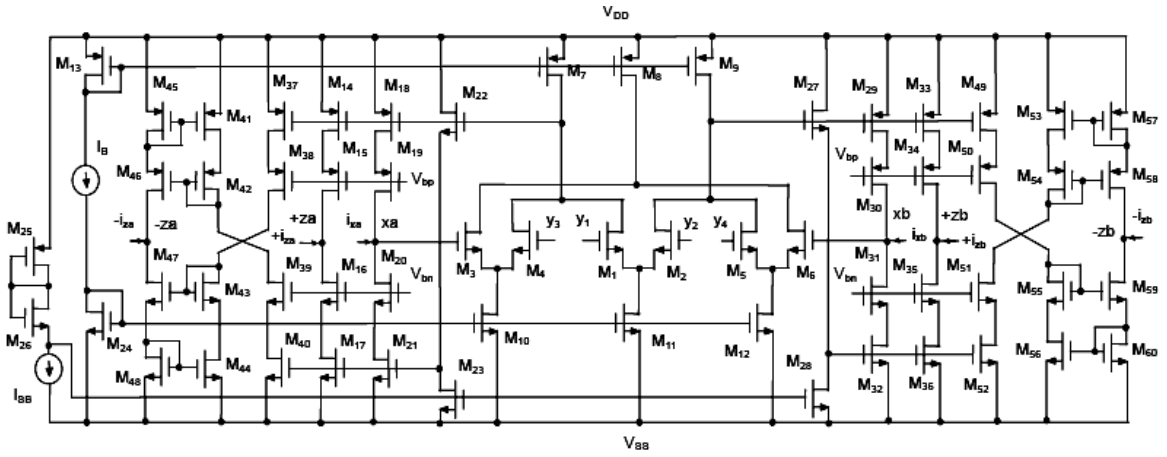

Figure 2. Cascode multiple outputs fully differential second generation current conveyor (FDCCII) [13]

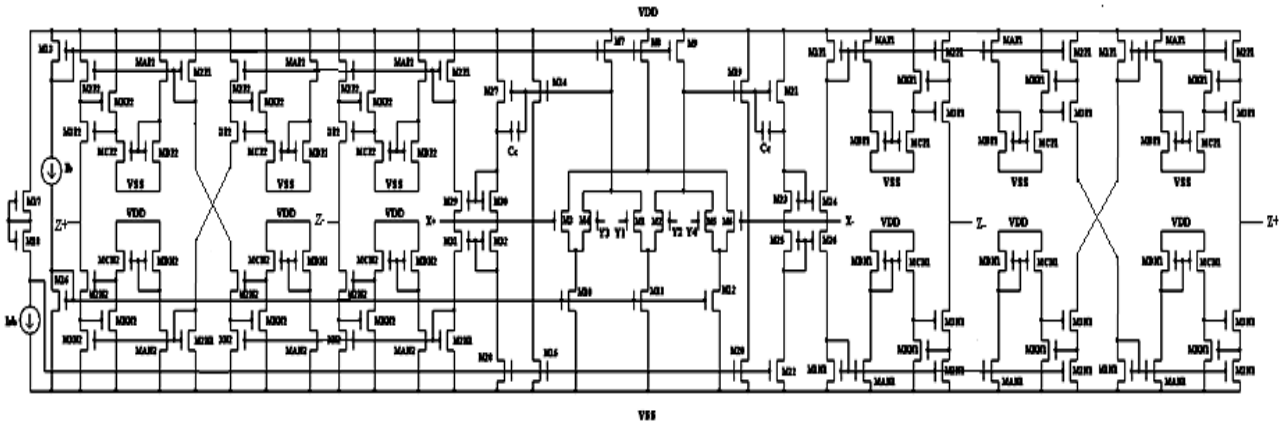

Figure 3. The proposed high performance mutiple outputs fully differential second generation current conveyor (FDCCII)

III. SIMULATION RESULTS AND COMPARISON

The performance of the proposed FDCCII is verified and compared with regular cascode FDCCII by SPICE simulation, using TSMC CMOS 0.35μm process model parameters for MOS transistors. Their aspect ratios are given in Table 1. The supply voltages, and biasing voltages, and currents are given by $V_{DD} = -V_{SS} = 1.25V$, $V_{bp} = -V_{bn} = 0V$, and $I_B = I_{SB} = 125$ μA, respectively.

The main dc and ac characteristics of the cascode and proposed high performance FDCCIIs, such as plots of V_X against V_Y, plots of $I_Z\pm$ against V_Y, frequency responses of V_X/V_Z and $I_Z\pm/I_X$ are obtained. The DC transfer characteristic of V_X against V_Y for the cascode and the proposed FDCCIIs are shown in Fig. 4. The input voltage is applied to terminal Y. The output voltage is then obtained at X, with an infinite load resistance connected at X; while output Z is grounded. The voltage limits at terminal X for the proposed FDCCII are obtained as: V_{Xmax}=390mV and V_{Xmin}=-390mV.

Figure 5 shows I_X-I_Z dc characteristics of the cascode and proposed FDCCII for short-circuited terminals X and Z. The lower and upper boundaries of the current I_Z for the proposed FDCCII are determined as: I_{Z+max}=0.8mA and I_{Z+min}= -0.8mA for positive Z terminal and negative Z terminal. The frequency responses of the voltage follower (V_X/V_Y) and current follower (I_Z/I_X) are shown in Figs. 6, and 7 respectively. The f_{3dB} frequencies for the proposed FDCCII are found as 2.02GHz and 2.15 GHz for V_X/V_Y, I_Z/I_X. The lower f_{-3dB} frequency for the voltage and current follower configurations in the proposed FDCCII stems from the higher output

resistance at terminal Z. However, it can be seen from Figs. 6 and 7 that the voltage and current gains for the proposed FDCCII are closer to unity, hence it has the higher accuracy.

The frequency responses of the output impedances at terminals Z for different types of FDCCII is shown in Fig. 8. The output resistances for the proposed FDCCII at terminals Z (impedances at low frequencies) are found as 577.68MΩ which are much higher than regular cascode FDCCII which has of value of 9.8MΩ

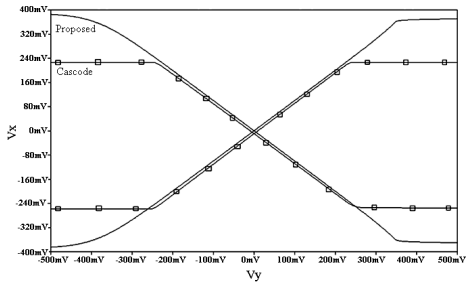

Figure 4. Relation between V_Y and V_X for cascode and proposed of FDCCII

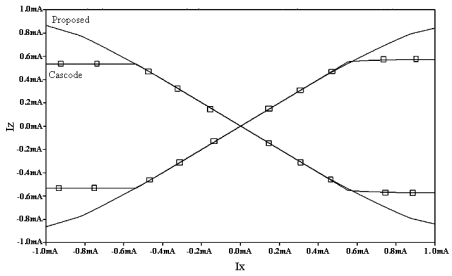

Figure 5. Relation between I_X and I_Z for cascode and proposed of FDCCII

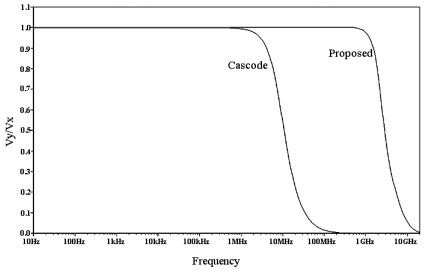

Figure 6. Frequency response of V_Y/V_X for cascode and proposed of FDCCII

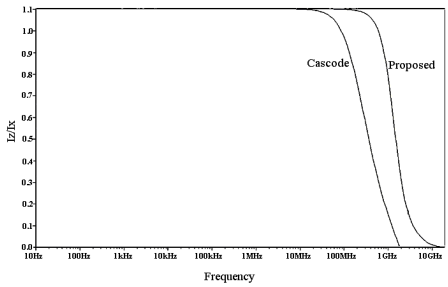

Figure 7. Frequency response of I_Z/I_X for cascode and proposed of FDCCII

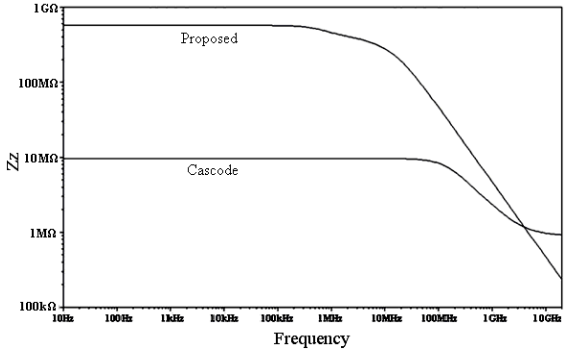

Figure 8. Frequency response of the output impedance at Z_Z terminal for cascode and proposed of FDCCII

Table.1 Transistors aspect ratios for the proposed circuit

Transistors	W(μm)	L(μm)
M_1-M_6, M_{BP},M_{CP}, M_{1N}-M_{3N}, M_{AN},M_{KN}	8.75	0.7
M_7-M_9,M_{13}	70	0.7
M_{10}-M_{12},M_{16}	17.5	0.7
M_{14},M_{15},M_{19},M_{20}	0.7	0.7
M_{17}, M_{21}, M_{27}, M_{25}-M_{26}, M_{31}-M_{32}, M_{1P}-M_{3P}, M_{AP},M_{KP}, M_{BN},M_{CN}	35	0.7
M_{18}, M_{22}-M_{24}, M_{28}-M_{30}	8.75	0.7
M_{31},M_{32}	105	0.7

IV. APPLICATION EXAMPLE AND SIMULATION RESULTS

As an application example, a CM multifunctional filter, shown in Fig. 9 [15] -with one input and three outputs- chosen from the literature is used to demonstrate the performance of the proposed FDCCII by replacing with previous ones.

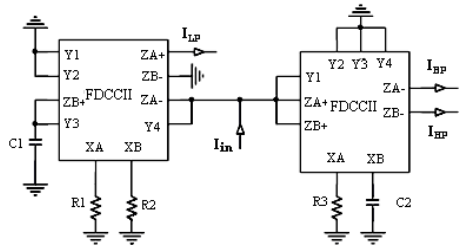

Figure 9. Universal current-mode multifunction filter [15]

Transfer functions are given as follows

$$\frac{I_{HP}}{I_{in}} = \frac{s^2}{s^2 + \frac{1}{R_3C_2}s + \frac{1}{R_1C_1R_2C_2}} \quad (4)$$

$$\frac{I_{BP}}{I_{in}} = \frac{\frac{1}{R_3C_2}s}{s^2 + \frac{1}{R_3C_2}s + \frac{1}{R_1C_1R_2C_2}} \quad (5)$$

$$\frac{I_{LP}}{I_{in}} = \frac{\frac{1}{R_1C_1R_2C_2}}{s^2 + \frac{1}{R_3C_2}s + \frac{1}{R_1C_1R_2C_2}} \quad (6)$$

The ω_o and Q are also given as follows.

$$\omega_0 = \sqrt{\frac{1}{R_1 C_1 R_2 C_2}} \qquad Q = R_3\sqrt{\frac{C_2}{R_1 C_1 R_2}} \tag{7}$$

The CM multifunction filter has been simulated using the SPICE program to verify the theoretical analyses. Simulated gain low-pass, band-pass, high-pass, amplitude-frequency responses are shown in Fig. 10. The resistance and the capacitance have been chosen as $R_1=R_2=R_3=22.5k\Omega$, $C_1=100pF$ and $C_2=50pF$, respectively for the pole frequency of *fo*=100 kHz. Since the Z output impedance is very high, the multifunction filter has very high output impedances, hence, the circuits are suitable for cascading when the Z terminal is connected to a current-mode circuit. To test the input dynamic rang of the proposed filters, the simulation of the band-pass filter as an example has been repeated for a sinusoidal input signal at *fo*≈100 kHz. Figure 11 shows that the input dynamic range of the filter response extends up to amplitude of 200 $\mu A_{(p\text{-}p)}$ without significant distortion. The dependence of the output harmonic distortion on the input signal amplitude is illustrated in Fig. 12.

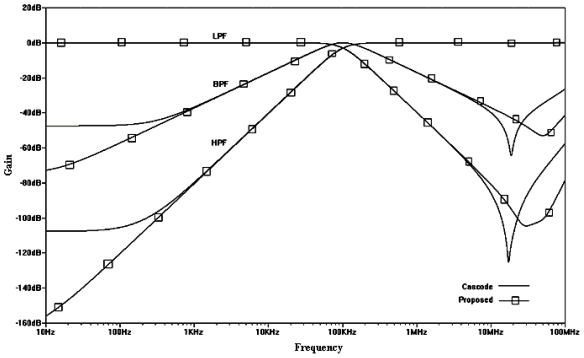

Figure 10. Frequency response of the current-mode filter (HP, BP, LP) for cascode and proposed of the FDCCII.

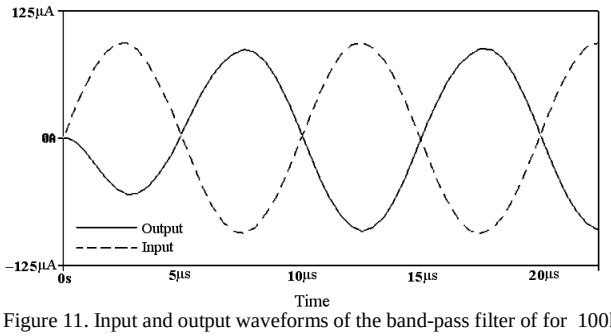

Figure 11. Input and output waveforms of the band-pass filter of for 100kHz sinusoidal input current of 200µA (peak to peak)

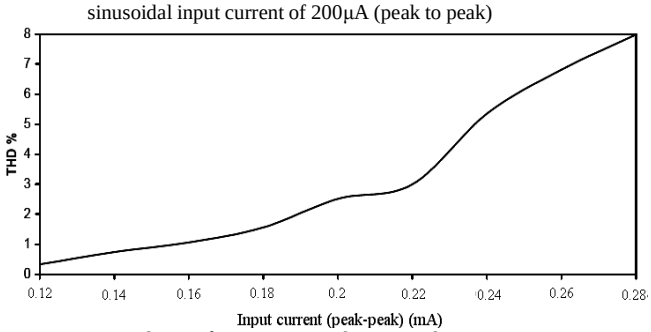

Figure 12. Dependence of output current harmonic distortion on input current amplitude of the proposed band-pass filter

V. CONCLUSION

A new high performance fully differential second-generation current conveyor FDCCII is presented. The proposed circuit uses improved active-feedback cascode current mirrors (IAFCCM), which significantly causes the output resistance at terminal Z to be higher than pervious ones. The circuit has a bandwidth of about 2 GHz under heavy capacitive loads and can operate with the supply voltages as low as ±1.25 V. The proposed block is also useful in mixed-mode applications where fully differential signal processing is required. By applying the proposed (FDCCII) to a chosen CM universal filter and by performing SPICE, the high performance capability and the versatility of the circuit are also demonstrated.

VI. REFERENCES

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