GaN Based Inverter Current-Collapse Behavior with Switching Frequency and Blocking Voltage

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***Abstract*—Current collapse in gallium nitride based transistors limit their use in high power and high frequency converters. In some cases, it makes the conduction losses to double. This paper investigates the measurement of dynamic on-state resistance for various cases such as blocking voltage and switching frequency. The optimum minimal length of pulses was determined in the case of three phase inverter to minimize the influence of current collapse.**

Keywords—GaN, current collapse, three phase inverter

I. Introduction

Gallium nitride (GaN) based transistors these days compete with silicon carbide (SiC) transistors in the field of power electronics. GaN transistors are dominant in middle voltage class up to 650 V while above that SiC transistors are available [1].

GaN transistors have lower switching losses compared to SiC due to the absence of substrate freewheeling diode. It means there is no recovery charge to limit the high frequency performance of GaN transistors. The absence of freewheeling diode is attractive for hard-switching circuits [2].

However, there are several issues that creates a challenge when using GaN transistors in power converters. The absence of freewheeling diode for example means the deadtime in half-bridge circuits needs to be minimized to prevent additional losses [3][4].

Another problem is the current-collapse phenomenon. The blocking voltage across the structure causes the on-resistance to be higher right after the turn-on compared to a steady state which is measured by manufacturers and listed in datasheets [5][6].

This on-state resistance increase is caused by higher gate threshold voltage of the transistor previously exposed to high blocking voltage [7].

The power loss caused by current-collapse also depends on the switching operation of transistor. It has more influence in hard-switching compared to soft-switching operation and the difference between them depends on temperature [8].

In this paper we focus on current-collapse increasing on-state resistance (R_{DSon}) of the GaN transistor in 3 phase motor inverter. The basic circuit is in Fig. 1.

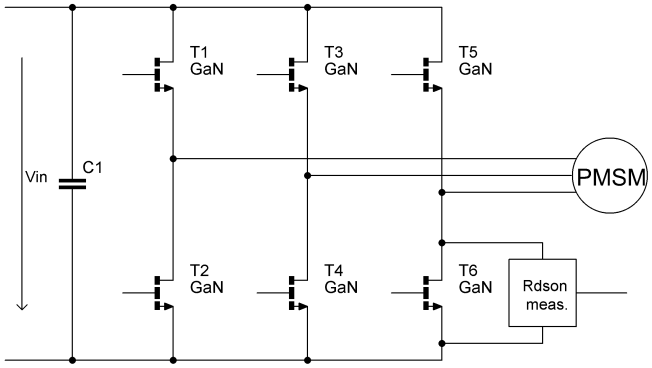

Fig. 1. Inverter topology

II. Theory

A. GaN Transistor

GaN based transistors used in power converters are lateral devices. The conduction channel is created by 2-dimensional electron gas (2DEG), that connects drain and source. The channel is located between AlGaN barrier layer and GaN buffer layer. Fig. 2 illustrates the structure of GaN based power transistor [9].

As shown above, a GaN device has no internal body diode. However, the device can operate in both directions. In forward mode when gate voltage is applied between gate and source, the channel is conducting the forward current. In reverse mode, device is opened by gate to drain voltage.

This type of operation increases the conduction losses in reverse mode and is called self-commutated reverse conduction mode [10].

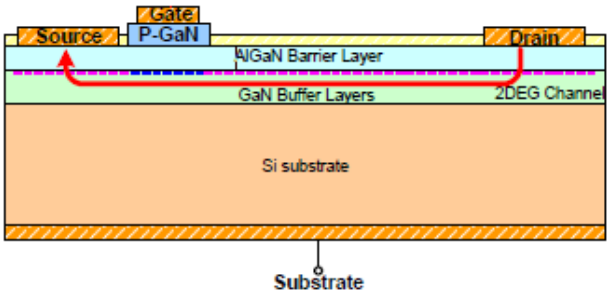

Fig. 2. Structure of GaN transistor [9]

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B. *Current Collapse Phenomenon*

Current collapse phenomenon is under-estimated due to representation of V-A characteristics. Standard V-A characteristics are measured for steady-state operation point.

The current collapse is taking place in switching period, when the device changes state from being turned-off to be turned-on. When the transistor is reverse biased, such as in off-state, electrons are injected into an available electron state either at the surface or the buffer layer of the device. When transistor is then switched on, the mobile charges are starting to conduct the current, whereas the trapped charges remain trapped for relatively long time of several microseconds. In this time the transistor has higher on-state resistance [11][12].

C. *Sampling circuit*

The drain to source voltage is sampled using depletion mode transistor. The circuit presented in [5] limits the amplitude when measured transistor is turned-off to about 3.3 V for the scope to be able to measure it precisely even at higher blocking voltages. When the measured transistor is turned-on the circuit enables to see the low voltage drop both positive and negative. It is because the sampling depletion mode field effect transistor is turned-on for both directions.

The circuit in Fig. 3 was adapted to a half-bridge and fitted into one leg of 3 phase GaN based inverter.

III. Experimental Setup

The experimental inverter power circuit is equipped with 6 GaN transistors GS66516B and fast isolated drivers Si8275. Each leg has its own high frequency C0G ceramic capacitor across DC-link to optimize the switching function.

As a main controller an ARM Cortex M4 MCU STM32F334 designed for power converters was used, which is equipped with a high resolution timer to precisely set deadtime and duty cycle at high switching frequencies. The sub 1 ns precision is important for fast switching GaN transistors to minimize the reverse conduction losses and also to achieve high enough resolution in duty cycle at high frequencies.

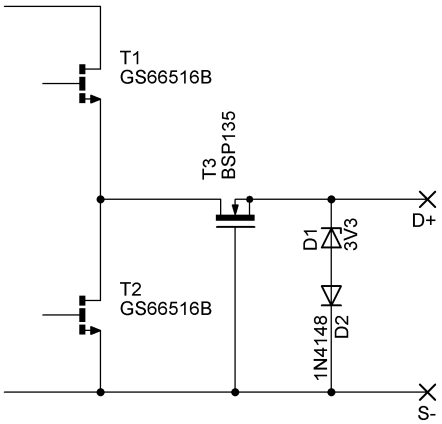

Fig. 3. Sampling circuit [5] on a half-bridge

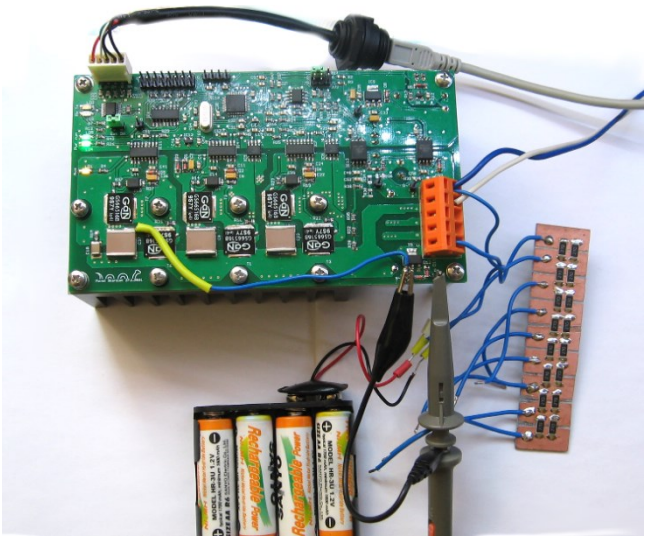

Fig. 4. Experimental setup with load resistor and bias battery

The integrated single board 3 phase inverter is shown in Fig. 4. The sampling circuit is fitted on the board in bottom right corner.

Since there are no freewheeling diodes present in the GaN transistor, the channel is used to conduct the reverse current instead. Because of this we have to perform measurements in both directions resulting in two channel resistances "Forward R_{DSon}" and "Reverse R_{DSon}".

To keep the constant current during the pulse it was measured at pure resistive load. For forward drain to source current the R_{DSon} was measured according to the schematic in Fig. 5. Small duty cycle limits the load resistor's dissipated power.

To measure the voltage drop in case of reverse current the circuit was reconfigured according to schematic in Fig. 6. The bias reverse current is provided by an external voltage source (battery) to minimize parasitic capacitances.

The inversed duty cycle again minimizes the dissipated power. The positive current pulse is always higher than the applied reverse bias current so the transistor is turned-off in the half-bridge circuit to be exposed to the measured input blocking voltage.

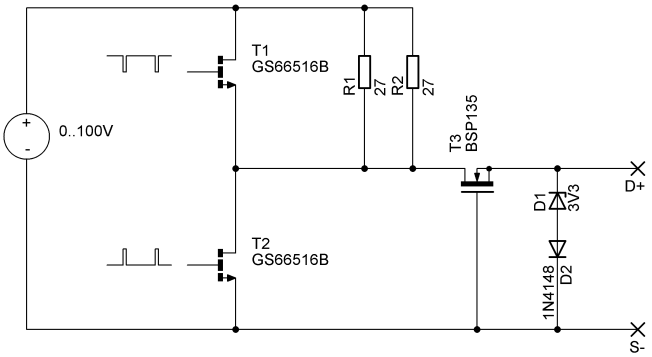

Fig. 5. Forward current measuring circuit

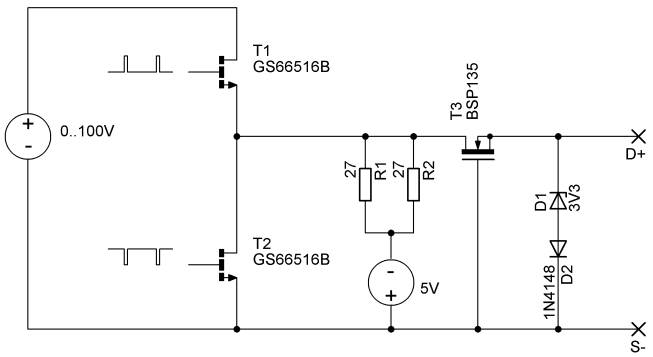

Fig. 6. Reverse current measuring circuit

The output of the sampling circuit in case of forward current is visible in Fig. 7 and in case of reverse current in Fig. 8. The measured pulse was 2 µs long out of 1 ms period in this case.

IV. Measured Data

The on-state resistance was measured for multiple values of blocking voltage and different length of pulses.

The R_{DSon} is calculated from the measured voltage drop on the sensing circuit and three different times 200 ns, 2 µs, and 20 µs. Fig. 9 shows the calculated values of R_{DSon} in case of forward current and Fig. 10 the calculated resistance when the transistor is switched on for the reverse current.

The set deadtime is 20 ns so the sampled value is taken at the time the transistor should be fully turned on by the positive gate to source voltage for the reverse current too.

Graphs show that the dynamic R_{DSon} is about twice as high as the static R_{DSon} listed in datasheet of GS66516 (25 mΩ) which corresponds with [5].

Fig. 11 shows the R_{DSon} plotted as a dependency on the length of pulse. This was calculated from the voltage drop caused by R_{DSon} at the end of the pulse of the given length representing the switching frequency.

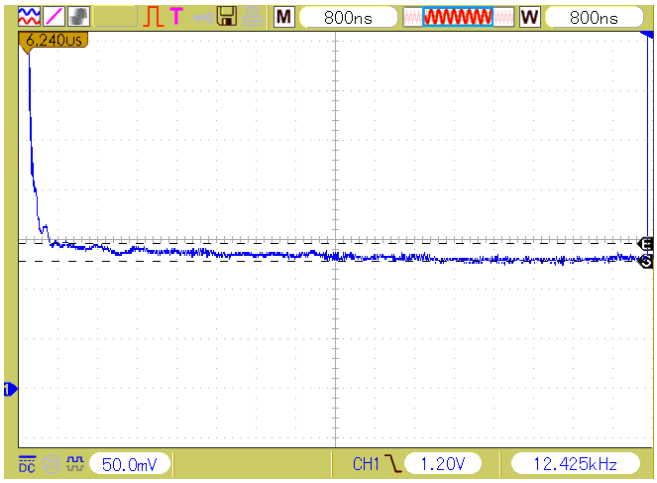

Fig. 7. Positive voltage drop after turn-on at forward current

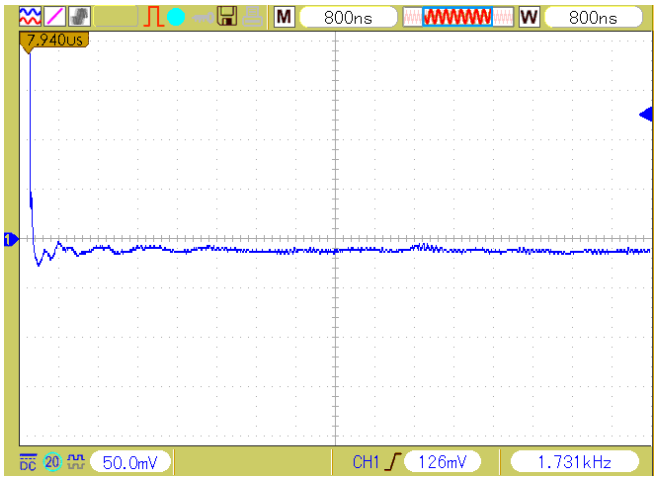

Fig. 8. Negative voltage drop after turn-on at reverse current

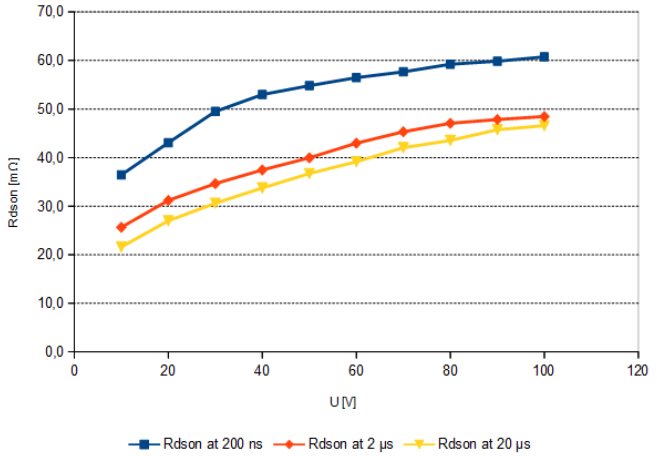

Fig. 9. Forward current R_{DSon}

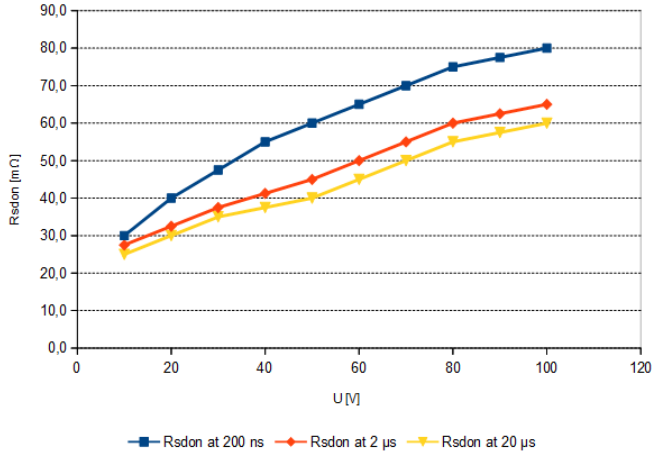

Fig. 10. Reverse current R_{DSon}

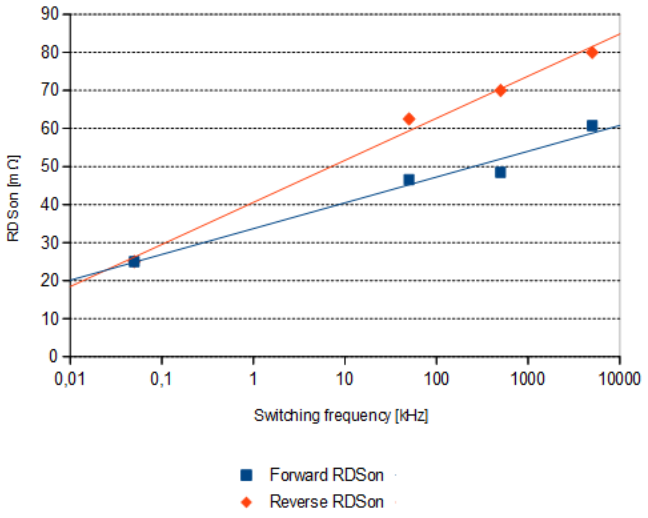

Fig. 11. R_{DSon} increase with switching frequency

It was also observed that the trapping process is very fast and changing turn-off time of the transistor is not making difference in the following turn-on pulse current-collapse effect which corresponds with [13].

To minimize the current-collapse losses in the inverter let's assume we want the dynamic R_{DSon} to be at maximum two times the listed datasheet value at the end of the shortest pulse modulating the inverter output voltage waveform. Based on measured results limiting the switching frequency below 100 kHz or 10 µs minimum on-time the dynamic R_{DSon} will be kept below 50 mΩ within the modulation period.

V. Conclusion

The current-collapse in GaN based semiconductors increases losses when converter transfers energy in short pulses such as low duty cycle at high voltage and high current, for example DC/DC converter with high input to output voltage ratio or voltage source inverter controlled by vector control around peaks of the sinusoidal modulation.

One solution is to limit the minimum on-time and decrease switching frequency at the small duty cycle. It can be easily implemented in the modulator of vector control. Measured results suggest also that fixed minimum switching time control schemes such as direct torque control or sliding mode control can perform better at reducing current-collapse introduced losses.

When designing a GaN based converter it is necessary to respect current-collapse when calculating power losses as it is present over the whole frequency range in which power converters are operating.

VI. Future Work

The control algorithm of the 3 phase inverter driving permanent magnet synchronous motor (PMSM) will be adjusted according to the measurements to achieve lower losses caused by the current-collapse phenomenon. Losses will be measured and comparison between multiple approaches minimizing them will be discussed.

Acknowledgment

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