LHC Clock Conditioning Circuit for AFP Trigger Module

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***Abstract* – The timing and synchronisation of the detectors in particle physics play the key role due to the high event rates at particle accelerators. The trigger module in ATLAS Forward Physics project selects the events from time of flight detector belonging to the proton bunch. As the time position of the proton bunch is the same within each Large Hadron Collider period, from the clock conditioning circuit (CCC) can be derived the qualification signal for the trigger module input signals. The further processing of these events in trigger module is allowed by the CCC qualification. High speed delay line integrated circuits together with the logic gates and FPGA based controller were used for the realization of the CCC. This paper describes the design, construction and test procedure of the CCC.**

Keywords – CERN, delay lines; high energy physics; LHC; particle accelerator; clock conditioning, physical instrumentation; synchronization; rad-hard

I. INTRODUCTION

The Large Hadron Collider (LHC) based in CERN is the largest circular particle accelerator worldwide with its 27 km circumference. There are five so-called interaction points at the LHC where the particle beams are collided. One of them is surrounded by the multipurpose ATLAS detector. The ATLAS Forward Proton (AFP) project extends the forward physics program of the ATLAS detector and is focused on the elastic proton-proton collisions [1]. The AFP project itself uses for its physical experiments two detectors: The *Time of Flight* (ToF) *detector* measures the momentum of the detected protons during the multiple p-p collisions. The *silicon tracking detector* measures the particle momentum of the diffracted protons. These particle detectors are symmetrically installed 210 m far from the ATLAS interaction point in both directions.

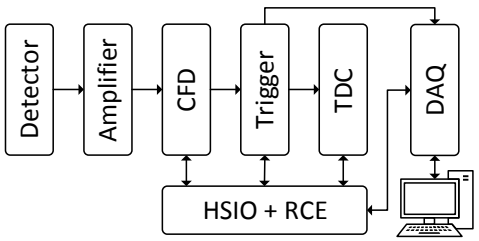

Figure 1. ToF detector [2]

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The ToF block diagram is shown in Fig. 1. The signals produced by the Cherenkov detector are then amplified and fed into the constant fraction discriminator module (CFD). This module converts the energy of the analog pulsed signals to the length of the digital pulses. The purpose of the Trigger Module (TM) is to decide whether the CFD signals fulfil the defined conditions and then the CFD signals pass through (or not) to the time time-to-digital (TDC) converter. The TDC converts the digital signals for offline computer data processing. The data collecting and control of the ToF chain is realized by the data acquisition (DAQ) and high-speed input/outputs (HSIOs) and reconfigurable cluster element (RCE) interface [3].

The LHC bunch clock f_{BC} is 40.08 MHz and the flying beam particles within each bunch are spread in the range of hundreds to thousands ps [4]. The purpose of the CCC is to define the time slot for the CFD output signals related to the particle bunches. This approach eliminates the unintentional processing of the CFD signals produced by the dark counts or any other disturbances inside the ToF detector.

The f_{BC} synchronization signal is distributed across the various facilities at LHC with using of the optical fibers and high-power laser transmitters. The received f_{BC} signal is then locally distributed within the defined facility (e.g. LHC experiment, test beam areas, LHC beam instrumentation etc.) [5].

II. DEVICE ARCHITECTURE

Before the design procedure started following specifications were defined:

- Tunable pulse width (from 400 ps to 10 ns)
- Settable delay (from 0 ns to 30 ns)
- Granularity of pulse width and delay <50 ps
- Temperature stability (1 °C hysteresis)
- Digital output temperature sensor
- Control circuit based on field-programmable gate array (FPGA)
- General purpose buttons and LEDs

The CCC architecture is depicted in Fig. 2. The f_{BC} for the TM is distributed in the current-mode logic (CML) standard (square signal, 50:50 duty cycle). The delay lines postpone the bunch clock signal. This delayed signal is then divided into two branches. One of them is directly connected to the two-input AND gate. The second branch delays and inverts the clock

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signal. The behavior of the whole circuit is known as a logic hazard and enables to create the pulses with the various length controlled by the delay circuit in the pulse width block. The fan-out buffer is then used to split the tuned bunch clock signal because of the five inputs of FPGAs inside the TM used for the CFD signal processing.

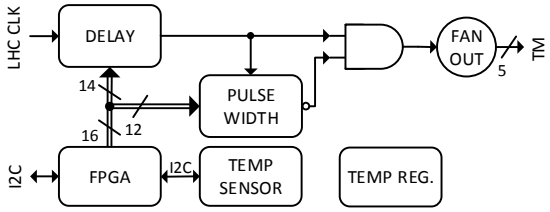

Figure 2. CCC architecture

The FPGA controls the delay lines, pulse width circuit and temperature sensor via two Inter-Integrated Circuit (I2C) buses. The internal bus is used for communication with the temperature sensor and in this case the FPGA is the master device. During the operation mode, the TM is a slave device for the TDC module and therefore the second (external) I2C bus is needed. Two general purposes buttons and four LEDs are also included in the circuitry.

As the commonly used delay line integrated circuits (ICs) are significantly temperature dependent the Peltier cell regulator is used to ensure the temperature stability.

III. Hardware Desciption

The majority of ToF electronics is installed near the LHC beam pipe and therefore only the radiation hardened and properly tested parts has to be used for the circuitry. The LHC clock in CML signal standard is ac-coupled to the CCC and then the low-voltage positive emitter-coupled logic (LVPECL) standard is used for the clock signal processing. The +3.3 low-voltage complementary metal oxide semiconductor (LVCMOS) signal levels are used for the control purposes and I2C communication.

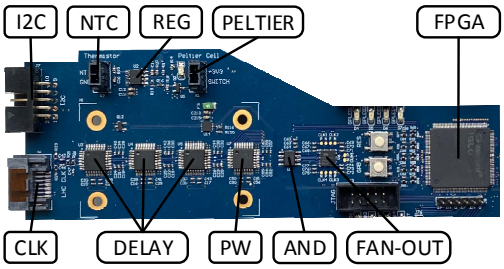

Figure 3. CCC PCB: regulator (REG), pulse width circuit (PW)

The CCC printed circuit board (PCB) is shown in Fig. 3. Differential traces with controlled impedance and length are used on the 6-layer PCB to ensure the signal integrity. The insulation-displacement contact (IDC) connector is used for I2C communication between the CCC and TDC module. The Serial AT Attachment (SATA) connector is commonly used for the LHC clock distribution at the ATLAS detector.

Four mounting holes surrounding the delay line ICs are used for mounting of the following stack: aluminum heat spreader, Peltier cell and heatsink. The negative temperature coefficient (NTC) thermistor is mounted on the heat spreader for closing of the temperature regulator feedback loop.

A. *Signal delay*

The CCC clock delay circuit consists of three serially connected delay lines MC100EP196 [6]. The delay of each IC is composed of the 2.4 ns fixed and 10.2 ns variable part for T = 25 °C. The ideal time granularity is 10 ps. The overall tunable delay is ranging from 0 ns to 30.6 ns.

B. *Pulse width*

The same type of delay line is used to postpone the delayed bunch clock signal on its way to the AND gate. In this case only one IC is used and therefore the variable delay is ranging from 0 ns to 10.2 ns. The required minimal pulse width (400 ps) is ensured by the proper matching of the PCB signal traces within the two branches leading the delayed bunch clock signal to the AND gate.

C. *Fan-out buffer*

Low-skew 1:8 fan-out buffer SY58033U is used to create five identical copies of the delayed clock signal with the tuned pulse width for the FGPAs used in the TM [7].

D. *Temperature sensor*

The two-channel sensor MCP9903 monitors the heat spreader temperature via internal I2C bus [8] with 1 °C accuracy and 0.25 °C resolution. One of the channels for the temperature measurement is inside the IC. The externally connected PNP transistor is used as the second channel.

E. *FPGA*

The FPGA M2GL005 belongs to the IGLOO2 family [9]. This IC is used for the CCC control due to its single-event upset immunity and the low power operation. Two general-purpose buttons are added to the FPGA together with four LEDs for diagnostic purposes.

F. *Temperature regulator*

As the propagation delay t_{PD} of the delay lines can vary significantly (9285 ps to 10875 ps are the typical values) over the IC operating temperature range (-40 °C to +85 °C) the constant temperature needs to be maintained [6].

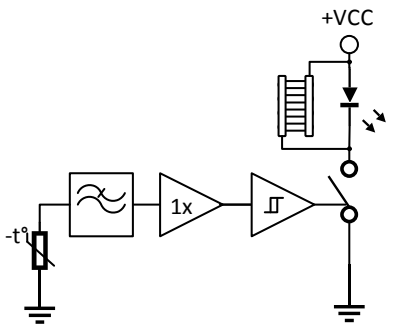

Figure 4. Temperature regulator for CCC

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As the power loss of the ICs leads to the heat spreader temperature rise only the cooling ability of the Peltier cell is sufficient in order to regulate the system temperature.

The temperature regulator used for the CCC is depicted in Fig. 4. The NTC thermistor is mounted on the heat spreader and senses its temperature. The RC low-pass filter includes also the pull-up resistor in order to create the voltage divider together with the thermistor. The filtered signal is then buffered by the voltage follower and connected to the inverting Schmitt trigger. The two-channel operational amplifier TLV2462 is used for the voltage buffering and comparing [10]. This circuit turns ON/OFF the switch (metal-oxide-semiconductor field-effect transistor) and thus controls the Peltier cell CP60340 [11]. The LED diode is also added for the diagnostic purposes.

The power loss of the delay lines heated the heat spreader to 46 °C during the long-term test. Due to this fact the Schmitt trigger levels correspond to the 44 °C and 45 °C as the ambient temperature in the LHC tunnel can affect the maximum temperature level of the heat spreader.

IV. FPGA Firmware

The CCC firmware is written in Very High-Speed Integrated Circuits Hardware Description Language (VHDL). After the code debugging and simulations in the ModelSim the Libero IDE was used for the code synthesis and implementation into the FPGA [12, 13].

The CCC architecture is shown in Fig. 5. The I2C slave entity transfers the data and commands between the CCC (slave) and TDC module (master). This entity also communicates with the finite state machine (FSM) in both directions.

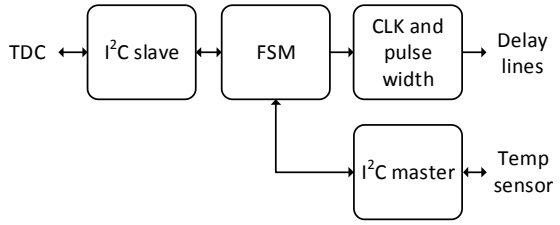

Figure 5. CCC firmware architecture

The FSM controls all the CCC circuitry. This entity uses the TDC commands to set clock signal delay and its pulse width. One of the other features is cyclically reading out the temperature from the I2C slave sensors (internal and external). The FSM also includes a few states (temperature sensor control, clock signal delay and pulse width settings) and data (internal and external temperatures, general purpose LEDs and buttons) registers.

V. Tests and Measurement

The MC100EP196 delay line IC datasheet defines the minimal, typical and maximal values of step delay for temperatures -40, +25 and +85 °C. As the operating temperature range of the delay IC is regulated and ranging from 44 °C to 45 °C, the step delays for these temperatures had to be defined. For obtaining the required values in Tab. I the polynomial regression (second order) was used. The D0-D9 bits can be set to the high (delay element activated) or low (not activated) level. The ideal set decimal value on the D0-D9 inputs multiplied by ten roughly corresponds to the IC propagation delay. The last line in the TABLE I. stands for the IC maximum delay (D0-D9 activated and one more gate delay element is included). This maximum delay is activated by the D10 pin and affects the previous IC in the signal delay chain.

TABLE I. DELAY LINE IC – PROPAGATION DELAYS

Bit Nr. [-]	Step delay					
	$\Delta t_{44°Cmin}$ [ps]	$\Delta t_{44°Ctyp}$ [ps]	$\Delta t_{44°Cmax}$ [ps]	$\Delta t_{45°Cmin}$ [ps]	$\Delta t_{45°Ctyp}$ [ps]	$\Delta t_{45°Cmax}$ [ps]
D0	11.3	11.3	11.3	11.3	11.3	11.3
D1	30.8	30.8	30.8	30.9	30.9	30.9
D2	49.3	49.3	49.3	49.4	49.4	49.4
D3	68.8	68.8	68.8	68.9	68.9	68.9
D4	102.7	153.1	205.4	102.9	153.3	205.7
D5	267.1	321.5	380.1	267.4	322	380.6
D6	575.2	646.1	729.3	576	647	730.3
D7	1160.7	1270.6	1391.9	1162.3	1272.4	1393.8
D8	2352.3	2539.2	2752.9	2355.5	2542.7	2756.6
D9	4714.8	5089.8	5531.5	4721.3	5096.7	5539
M[a]	9344	10192	11162	9357	10206	11178

a. D0-D9 bits set high & 1 element with t_{PD_D0} added.

During the CCC circuit testing the real pulse width and signal delays vs. the set values were measured and plotted in Fig. 6 and 7. The Calc_min and Calc_max lines correspond to the $\Delta t_{44°Cmin}$ and $\Delta t_{45°Cmax}$ as the step delay can vary between these two limits during the temperature regulation. The mean value of 64 samples for each of the data points in Fig. 6 and 7 was collected.

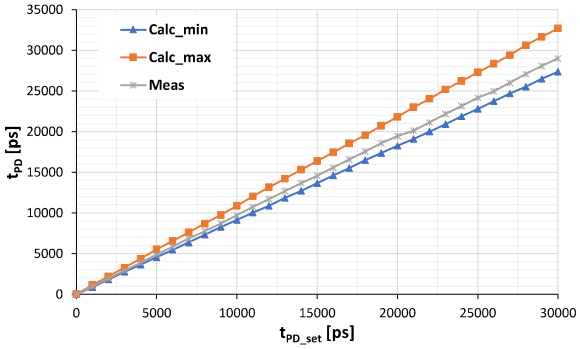

Figure 6. Clock signal propagation delay (measured, calculated limits) vs ideal set value

The clock signal propagation delay function depicted in Fig. 6 is ranging from the 0 ps to 30 ns. 1000 ps steps were gradually set and the t_{PD} was measured. The measured values are inside the calculated limits for the operating temperature range.

The signal pulse width values shown in Fig. 7 are also in the calculated range. The 250 ps steps were used for the measurement. The pulse width offset caused intentionally by the PCB signal trace delay was measured as 387 ps.

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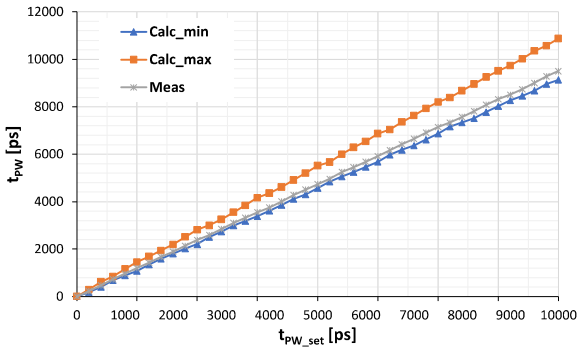

Figure 7. Clock signal pulse width (measured, calculated limits) vs ideal set value

The two-channel temperature sensor was active during the measurement and signalized the CCC operating temperature within the defined boundaries via diagnostic LED. This feature used internal and external temperature values compared to the lower (44 °C) and upper (45 °C) thresholds.

As a master device for sending the commands to the CCC and reading out the temperatures the Raspberry Pi was used. A simple Python script cyclically tested the pulse width and signal delay features of the circuitry with the finest granularity possible (10 ps).

The thermocouple was used during the CCC test to monitor the proper function of the Peltier cell temperature regulator. The 1.2 °C wide hysteresis was observed.

The signal generator SRS SG382 sourced the 40.08 MHz square wave signal to the CCC during the tests [14]. The pulse width and signal delay were measured by the oscilloscope MSOS804 together with the active differential probes U1818B [15], [16].

VI. Conclusion

The tests of CCC circuitry proved the ability to set the pulse width and delay of the LHC clock signal in the required range. The obtained values meet the specified calculated limits. The functions of the measured pulse width and delay vs the ideal set values are strongly linear as expected.

The proper operation of the I2C temperature sensor has been also verified as well as the temperature regulation.

The CCC will be implemented in the next generation of the TM. This module will be then tested at the synchrotron in DESY (Hamburg) and installed at the LHC in CERN.

Acknowledgment

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References

[1] S. Grinstein on behalf of AFP Collaboration, "The ATLAS Forward Proton Detector (AFP)," in Nuclear and Particle Physics Proceedings, Science Direct, vol. 273-275, April-June 2016, pp. 1180–1184.

[2] J. Zich et. al., "Multichannel Coincidence Circuit with Settable Threshold Level for ToF AFP Detector," in 27 Telecommunications forum TELFOR 2019, Belgrade, Serbia, 2019, pp. 1-4.

[3] R. Bartoldus et. al., "A new ATLAS muon CSC readout system with system on chip technology on ATCA platform," in Journal of Instrumentation 11, 2016.

[4] B. G. Taylor, "Timing distribution at the LHC," in Workshop on Electronics for LHC Experiments, September 2002.

[5] J. Varela, "Timing and synchronization in the LHC experiment," in Workshop for Electronics for LHC Experiments, September 2000.

[6] "MC100EP196 delay line datasheet," ON Semiconductor, Worldwide, 2014, Available: https://www.onsemi.com/pub/Collateral/MC100EP196-D.PDF.

[7] "SY58033U fanout buffer datasheet," Micrel, Worldwide, 2011, Available: http://ww1.microchip.com/downloads/en/DeviceDoc/sy58033u.pdf.

[8] "MCP9903T temperature sensor datasheet," Microchip, Worldwide, 2015, Available: https://ww1.microchip.com/downloads/en/DeviceDoc/20005382C.pdf.

[9] "IGLOO2 FPGAs," Microsemi, Worldwide, 2019, Available: https://www.microsemi.com/product-directory/fpgas/1688-igloo2.

[10] "TLV2462 operational amplifier datasheet," Texas Instruments, Worldwide, 2020, Available: https://www.ti.com/lit/ds/symlink/tlv2462a-ep.pdf?ts=1591121078831.

[11] "CP60340 peltier cell datasheet," CUI devices, Worldwide, 2020, Available: https://www.cuidevices.com/product/resource/cp60.pdf.

[12] "ModelSim," Mentor, Worldwide, 2020, Available: https://www.mentor.com/products/fv/modelsim/.

[13] "Libero SoC v12.0," Microsemi, Worldwide, 2020, Available: https://www.microsemi.com/product-directory/design-resources/1750-libero-soc.

[14] "SG382 RF signal generator," *Keysight Technologies*, Worldwide, 2019, Available: https://www.thinksrs.com/products/sg380.html

[15] "MSOS804 High-Def Oscilloscope," *Keysight Technologies*, Worldwide, 2019, Available: https://www.keysight.com/en/pdx-x202079-pn-MSOS804A.

[16] "U1818B Active Diff. Probe," *Keysight Technologies*, Worldwide, 2019, Available: https://www.keysight.com/en/pd-1729219-pn-U1818B.

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