New Input Offset Voltage Measurement Setup for Ultra Low-Voltage Fully Differential Amplifier

Miroslav Potočný, Michal Šovčík, Daniel Arbet, Viera Stopjaková and Martin Kováč

Department of IC Design and Test
Faculty of Electrical Engineering and Information Technology
Slovak University of Technology
Bratislava, Slovakia
e-mail: miroslav.potocny@stuba.sk

***Abstract*—This paper deals with the measurement of input offset voltage of a fully differential low–voltage variable gain amplifier intended for on–chip systems. A new measurement setup that effectively separates the output common and differential mode signals was developed. By only using the differential output voltage in the feedback path, any common mode errors are effectively suppressed. As the gain of the device to be measured was expected to be relatively low, an auxiliary loop amplifier was introduced in each feedback path to increase the loop gain of the circuit as well as reduce loading of the device under test. This effectively reduces measurement errors caused by the non–ideal parameters of the device under test. A test board was developed and verified by the measurement of bare–die samples. Slight deviation of results when compared to simulated data was observed. This is likely due to the use of probe needles, which results in varying contact quality and a rather small number of samples available for measurement.**

Keywords—measurement; input offset voltage; fully differential amplifier; ultra low-voltage

I. Introduction

The operation of a precise analog circuit greatly depends on the matching of differential paths. However, current down–scaled process technologies suffer from significant deviations of process parameters. According to [1], the standard deviation of the transistor threshold voltage (V_{TH}) in $45\ nm$ CMOS process node reaches approximately $16\ \%$ of the mean value. Such a mismatch in the differential structure of an operational amplifier is the origin of the input offset voltage. This undesired parameter is tightly related to the degradation of other AC or DC amplifier parameters or, in other words, to the decrease of IC production yield. Therefore, the measurement of this parameter is of great importance. The reduction of the supply voltage in these circuits brings new challenges related to the measurement of such parameters, which is the main focus of this paper.

This paper is structured as follows: Section 2 gives a summary of DC errors in a fully differential amplifier (FDA) with external feedback. Section 3 gives a brief description of the device under test (DUT) used for the measurement. Section 4 deals with the proposed differential measurement method and gives examples of single ended methods from which it was adapted. Section 5 presents the measured results and gives a comparison to simulated data. Section 6 gives a brief summary of the achieved results.

II. DC errors in a FDA with external feedback

Sources of DC errors in a FDA amplifier with external feedback depicted in Fig. 1 can be summarized as [2]:

- input offset voltage (V_{IO})
- input bias current (I_{IB})
- input offset current (I_{IO})
- input and output common–mode mismatch ($V_{OCM} - V_{ICM}$)
- input common–mode and power supply rejection ratios ($CMRR, PSRR$)
- feedback non–symmetry (β_1, β_2)

Parameters b_1 and b_2, given by Eq.1 and Eq. 2, are dependent on the CMRR value (of the FDA). The two feedback paths are characterized by parameters $\beta_1, \beta_2, R_{EQ1}$ and R_{EQ2}, as described by Eq. 3–6. The parameter A in these equations is the open loop gain of the amplifier. The resulting DC output voltage is defined by Eq. 7–12. These equations describe the desired signal V_{OD} and the error voltage ΔV_{OD} caused by $V_{IO}, I_{IB}, I_{IO}, V_{OCM}, V_{ICM}$, and the input common mode V_{ICM} and power supply ripple V_{EPS} voltages, in this order.

$$b_1 = 1 + \frac{1}{2CMRR} \tag{1}$$

$$b_2 = 1 - \frac{1}{2CMRR} \tag{2}$$

$$\beta_1 = \frac{R_{F1}}{R_{F1} + R_{G1}} \tag{3}$$

$$\beta_2 = \frac{R_{F2}}{R_{F2} + R_{G2}} \tag{4}$$

ISBN 978-80-261-0722-4,

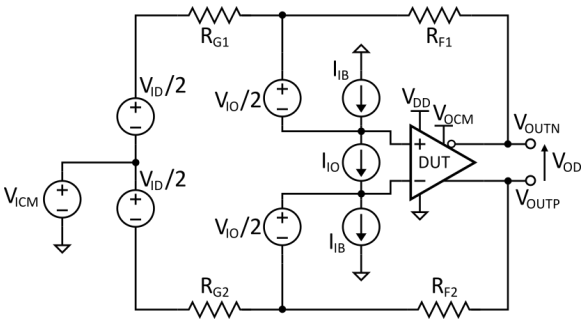

Fig. 1. Sources of DC errors in a FDA with external feedback [2].

$$R_{EQ1} = \frac{R_{F1}R_{G1}}{R_{F1} + R_{G1}} \tag{5}$$

$$R_{EQ2} = \frac{R_{F2}R_{G2}}{R_{F2} + R_{G2}} \tag{6}$$

$$V_{OD} = V_{ID}\frac{2 - (\beta_1 + \beta_2) - \frac{(\beta_1 - \beta_2)}{2CMRR}}{(\beta_1 + \beta_2) + \frac{(\beta_1 - \beta_2)}{2CMRR} + \frac{2}{A}} \tag{7}$$

$$\Delta V_{OD}(V_{IO}) = V_{IO}\frac{b_1 + b_2}{b_1\beta_1 + b_2\beta_2 + \frac{2}{A}} \tag{8}$$

$$\Delta V_{OD}(I_{IB}) = 2I_{IB}\frac{b_1R_{EQ1} - b_2R_{EQ2}}{(b_1\beta_1 + b_2\beta_2) + \frac{2}{A}} \tag{9}$$

$$\Delta V_{OD}(I_{IO}) = I_{IO}\frac{b_1R_{EQ1} + b_2R_{EQ2}}{(b_1\beta_1 + b_2\beta_2) + \frac{2}{A}} \tag{10}$$

$$\Delta V_{OD}(V_{OCM}, V_{ICM}) = \\ = \frac{2(V_{OCM} - V_{ICM})(b_1\beta_1 - b_2\beta_2)}{(b_1\beta_1 + b_2\beta_2) + \frac{2}{A}} \tag{11}$$

$$\Delta V_{OD}(V_{ICM}, V_{EPS}) = \frac{\frac{2V_{ICM}}{CMRR} + \frac{2V_{EPS}}{PSRR}}{(b_1\beta_1 + b_2\beta_2) + \frac{2}{A}} \tag{12}$$

If we assume that all sources of DC errors except for V_{IO} are negligible, the gain of the FDA is very large, and the two feedback paths are perfectly symmetrical (e.g. $R_{G1} = R_{G2} = R_G, R_{F1} = R_{F2} = R_F, A \Rightarrow \infty$) we can simplify the gain of the network, when considering V_{IO} as the input voltage (Eq.13), which is also known as the amplifier noise gain [2].

$$\frac{\Delta V_{OD}(V_{IO})}{V_{IO}} = \frac{R_F + R_G}{R_G} \tag{13}$$

The accuracy of this simplification depends on parameters of the device under test (DUT), most notably its open-loop gain. This parameter has to be large enough to ensure that the close-loop gain is only dependent on the feedback path and not the gain of the DUT. This is similar in principle to the commonly used closed-loop gain (A_{CL}) equation in single ended amplifiers given by Eg. 14, where A_{OL} is the open-loop gain of the amplifier and β is the gain of the feedback. This also simplifies to $A_{CL} \cong 1/\beta$ under the assumption that $A_{OL} \gg \beta$ and $A_{OL}\beta \gg 1$. This is not always achievable with low-voltage devices, as will be discussed in Section 3. Therefore, a measurement circuit for such devices needs to increase the loop gain of the system, generally by using an auxiliary amplifier in the feedback loop.

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta} \tag{14}$$

Further steps have been taken in the design of the measurement circuit to minimize all other sources of voltage errors, except for V_{IO}. Among others, these steps include the use of a stabilized battery powered supply, the use of precision circuit elements, or design of the PCB signal traces to be as symmetrical as possible. These will be described in more detail in Section 4.

III. Device Under Test

An ultra-low voltage two-stage VGA has been used as the DUT. Fig. 2 shows its block diagram. The first stage is formed by a variable–gain differential difference amplifier (DDA) designed using the bulk–driven (BD) approach. The second stage has a fixed gain and is created by a BD common–source amplifier (CSA). A similar ultra–low voltage VGA was presented in [3], [4]. For stabilization of the operational point of both stages, two BD common–mode feedback (CMFB) circuits were used. To achieve good stability of the CMFB loop and the whole two–stage VGA, frequency compensation circuitry has been employed. The DUT was designed to operate with the power supply voltage of 600 mV. Preliminary testing revealed that the CMFB circuits did not achieve enough gain to accurately set the V_{OCM}, resulting in rather large common–mode mismatch between V_{OCM} and V_{ICM}. A circuit that would separate this common–mode error from the differential–mode error voltage was therefore needed for the measurement of V_{IO}.

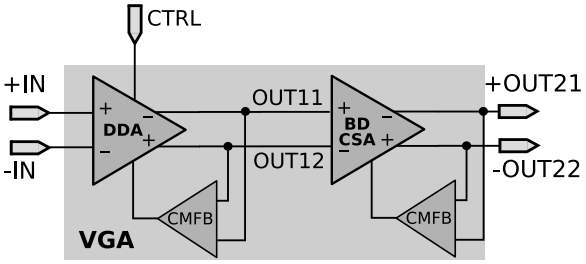

Fig. 2. Block diagram of the VGA used as DUT.

The frequency response of the DUT obtained by simulation and measurement is shown in Fig. 3. The range defining the minimum and maximum values of the gain was obtained from Monte Carlo (MC) analysis, where the process variation and mismatch of all devices ($\pm 3\sigma$) were taken into account. The measured frequency response was obtained by measurement of a single packaged prototype chip at the temperature of 27°C. It can be observed that the measured frequency response slightly deviates from the mean frequency

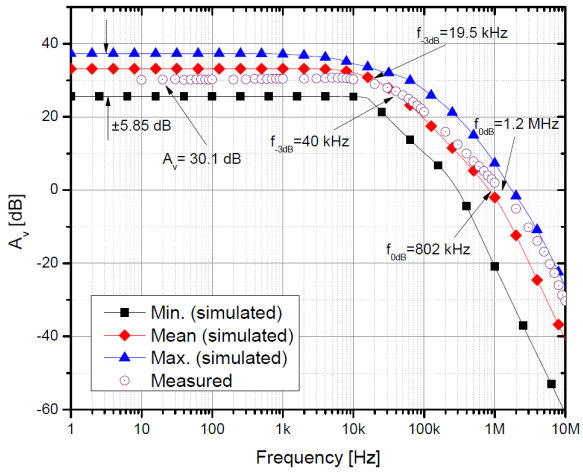

Fig. 3. Frequency response of the VGA.

response obtained by MC analysis. The results were measured and compared for the control voltage of 100 mV and load capacitance of 10 pF. For these conditions, the measured VGA gain is about 30 dB and the gain bandwidth of 1.2 MHz was achieved. The value of bandwidth is 40 kHz.

Since the input offset voltage of the DUT should be measured in a closed-loop configuration, the gain error introduced by the finite gain of the DUT has to be investigated. The desired gain, as described by Eq. (13), was set to 11 (e.g. $R_F = 10R_G$). The actual gain of the circuit, calculated from Eg. 8 is 8.25, which is roughly 33 % below the gain set by the feedback resistors. This is an unacceptably large error, caused by the low value of the loop gain ($A_{OL}\beta \approx 1$). This value would also fluctuate on each device, making consistent measurement impossible without previously measured DC open-loop gain of each DUT. Therefore, an additional amplifier had to be employed to increase the overall loop gain of the circuit and make the output voltage independent on the DUT open-loop gain.

IV. Input Offset Measurement Techniques

A. Related work

There have been limited number of papers found related to the input offset measurement of a fully differential amplifiers. Therefore, we looked at solutions for single-ended devices as well. A method utilizing an external operational amplifier (OA) in the feedback loop [5] is a relatively simple and precise measurement technique. The additional loop amplifier has its non–inverting input referenced to the ground (or mid–supply in single supply applications), as shown in Fig. 4. Thus, when the loop is closed, the output of the DUT is forced to ground by the negative feedback realized by resistors R2 and R4. These two resistors also set the gain of the system that is given by Eq. 15. R1 has a value identical to R2 value and negates the effect of the common–mode portion of the input bias currents. The addition of the loop amplifier rises the loop gain of the system, making it less dependent on the gain of the DUT. This is very useful for the measurement of low–voltage devices, where lower open-loop gain is to be expected (as mentioned in Section 3). Also the DUT only has to drive the input of the loop amplifier, therefore any loading related degradation of its parameters can be assumed to be insignificant.

$$\frac{V_{OUT}}{V_{IO}} = \frac{R2 + R4}{R2} \tag{15}$$

The major disadvantage of this method is its inherent instability, as the auxiliary OA is part of the DUT feedback. The frequency response of the loop amplifier increases the loop gain magnitude and introduces additional phase shift, effectively reducing the phase and magnitude margins and potentially causing oscillations. Nevertheless, the addition of R3 and C1 turns the loop amplifier into an integrator and improves the stability of the system. The values of these two circuit elements need to be adjusted ad–hoc, as the potential oscillation frequencies change depending on the open-loop frequency responses of the DUT and OA used. Recently, a test measurement board based on this approach was presented in [6], where satisfactory precision was reported. A modified method of this circuit can be found in [7] or [8], where an additional buffer amplifier was introduced into the loop, providing more control over the final loop gain (this is also know as a servo loop). This makes adjustments and stabilization of the whole circuit easier.

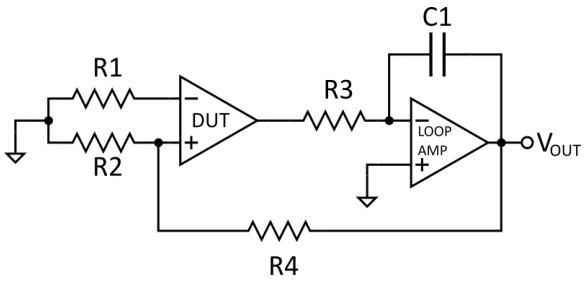

Fig. 4. Single-ended amplifier input offset voltage measurement configuration using an auxiliary loop amplifier.

B. Proposed measurement circuit

The methods discussed above cannot be straightforwardly employed for the DUT just by a simple use two loop amplifiers, one in each feedback path. If the loop amplifier inputs are referenced to the same common mode voltage as the DUT input, any mismatch of the output and input common mode voltages of the DUT would also be included in the feedback signal. This results in an additional error voltage, as defined by Eq. 11, which is not caused by the V_{IO}. To separate the common mode and the differential parts of the output signal, both inputs of the loop amplifiers are driven by the DUT inverting and non–inverting outputs, effectively suppressing any common mode error of the DUT. This also effectively doubles the gain set by the feedback resistor network (Eq. 13) due to using the whole V_{OD} amplitude in both feedback paths, as opposed to half in each one of them, as was the case in the circuit in Fig. 1.

To make this approach possible we need to be able to set the output common mode voltage of the loop amplifiers to the same voltage as the input common–mode voltage of the DUT. Therefore, we chose to use

instrumentation amplifiers (instead of simple OAs) as the auxiliary loop amplifiers. This also allows the loop gain of the system to be adjusted without changing the impedance seen by the DUT output, giving us more control over the feedback loop as a whole. Replacing the two loop amplifiers by an auxiliary FDA was also considered. Such devices have worse DC performance when compared to purpose designed high DC precision instrumentation amplifiers, which is the reason this idea was ultimately rejected. We chose the Analog Devices AD8237 as the loop amplifier. This is a rail-to-rail, low-voltage, excellent DC performance instrumentation amplifier [9] that suited our needs very well. It is capable to operate with a single supply voltage as low as 1.8 V, which reduces the risk of damaging the low-voltage DUT if any unforeseen oscillations were to occur. Its major drawbacks include a relatively low bandwidth (BW) and possible transient noise from the internal level shifting circuitry. These are of little concern when conducting pure DC measurements and thus, can be ignored. The low BW of the device turned out to be of benefit in this application, as it limits the possibility of high frequency oscillations in the loop.

A simplified schematic of the proposed measurement circuit is shown in Fig. 5. The output and input common-mode voltages of the DUT and loop amplifiers were set to half of the DUT supply voltage. This effectively eliminated the mismatch between V_{ICM} and V_{OCM} and thus, the error voltage (11). The whole setup was powered by a Zener diode stabilized adjustable battery source that provided the necessary supply and control voltages for the DUT and loop amplifiers. A single 9 V battery was used as the power supply. This was done to minimize noise in these signals and make the output error voltage due to the DUT PSRR parameter (Eq.12) negligible. Capacitor C_C was used to reduce the differential output noise and BW of the DUT, without the degradation of its DC performance. This also improved the stability of the circuit to the point where no other stabilization circuitry was necessary. The gain of the DUT was set to its maximum value, to minimize DC gain errors.

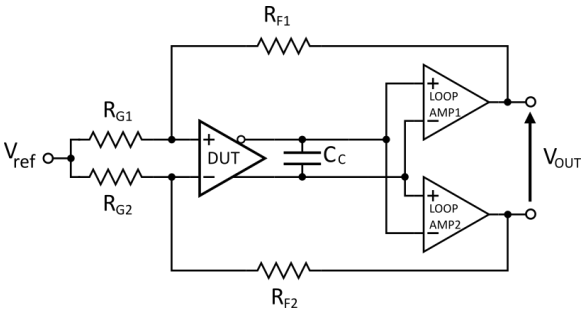

Fig. 5. Simplified schematic of the proposed measurement circuit.

A test board including the above mentioned circuitry was manufactured. The resistors used in the feedback networks and as gain setting resistors for the loop amplifiers all have 0.1 % tolerances, to minimize any non–symmetry of the feedback paths. This makes parameters $\beta_1, \beta_2, R_{EQ1}$ and R_{EQ2} (Eq. 3–6) as close to equal as possible, minimizing the error voltage from I_{IB}(Eq. 9), as well as the error their mismatch introduces into Eq. 7–12.

The gain of the circuit was set to be 22, giving us an expected differential output voltage in tens of millivolts. This ensures that the DUT operates within its linear region, which is rather limited by its very low supply voltage of 0.6 V. Larger gains were considered to make the output easier to measure but this caused the loop to be unstable. The test board was intended to be used with conjunction with an integrated circuit probe station to perform bare–die device measurement. Therefore, BNC–type coaxial connectors were added to provide connections to the probe needle manipulators. A photograph of the test board is shown in Fig. 6 and the whole measurement setup, including the probe station, is depicted in Fig. 7. The signal traces on the PCB were drawn as symmetrical as was possible, to make any parasitics equal in both feedback paths. The unused SMD pads are intended for further stabilization elements that were not needed in the end.

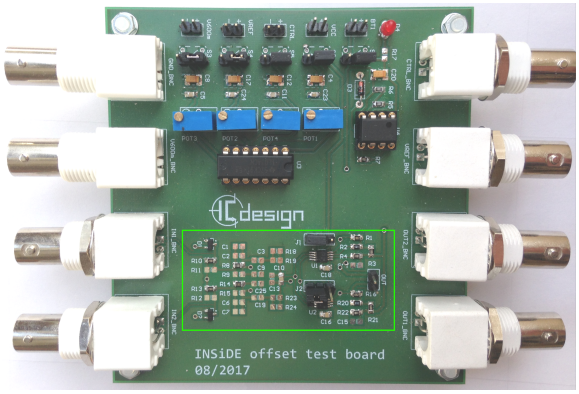

Fig. 6. The test board for measurement of the DUT input offset voltage.

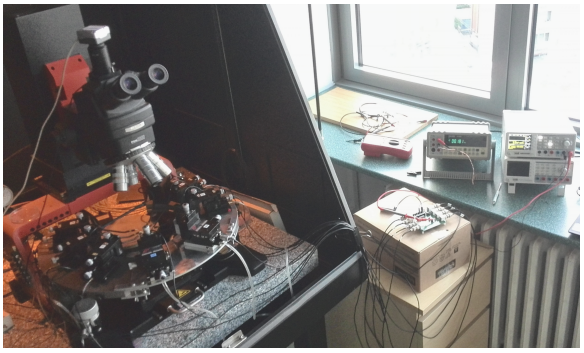

Fig. 7. Measurement of unpackaged sample dies using a probe station.

V. Achieved Results

Since additional circuitry was used for the measurement of V_{IO}, it was essential to determine its DC error voltage, which is obviously added to the measured results. The test board also adds a certain small error. However, as the measured input offset spans over just a few millivolts, even a small additional error could represent a substantial systematic discrepancy in the measurement results. Calibration measurement of the test board reveals that it adds a differential DC error of only $0.61\ mV$ to the DUT inputs. The relative gain mismatch of the two feedback paths was below 1 %, and could therefore be neglected.

Fig. 8 displays the comparison of the input offset voltage results obtained by simulation and measurement. The measurement was performed on unpackaged dies of 60 samples. The presented results take into account the test board DC error. The measured distribution's mean value μ reaches $403\ \mu V$ with a standard deviation σ of $3.45\ mV$. Simulated offset distribution exhibits $\mu = 131.5\ \mu V$ and $\sigma = 2.69\ mV$. Monte Carlo simulation with 500 samples was used. Due to the use of different numbers of samples in the measurement and simulation, the plots in Fig. 8 were normalized.

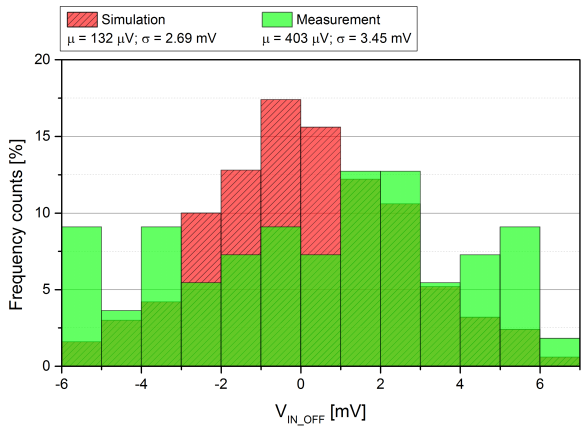

Fig. 8. VGA input offset statistical results: simulation vs measurement.

From the presented comparison (Fig. 8), a minor discrepancy can be observed. On one hand, this could be caused by rather small number of samples in the measurement. Acquired results' distribution would be most likely different, if few hundreds of samples were used. On the other hand, because the measurement used unpackaged dies contacted with probe needles, the quality of the contacts did likely fluctuate, causing additional errors in the measurement.

VI. Conclusion

A new circuit for the measurement of the input offset voltage of low–voltage FDAs was proposed. It utilizes two loop amplifiers to raise the loop gain of the system and make the resulting gain of the circuit independent of the DUT gain value. This allows rather precise measurement of low–gain circuits, such as the VGA used in our work. The proposed circuit utilizes only the differential output voltage of the DUT as the feedback signal. This effectively suppresses common–mode errors on the DUT output, which improve the accuracy of the measurement. The achieved measured results correlate very well with the results obtained by simulation. Occurred discrepancies are likely caused by the rather small sample size of 60 and the use of probe needles. The main disadvantage of this method is the inherent instability of the circuit. Careful design of the stabilization circuitry is therefore of great importance. Further improvements of this circuit could include the addition of capacitive compensation of the loop amplifiers, turning them into very low frequency integrators. Adding the ability to measure parameters such as the input bias current, CMRR, PSRR, and others, would also be a major improvement to the circuit and will be considered in the future.

Acknowledgement

This work was supported by the Ministry of Education, Science, Research and Sport of the Slovak Republic under grants VEGA 1/0762/16 and VEGA 1/0905/17, and by the Research and Development Agency under grant APVV-15-0254.

References

[1] M. Onabajo and J. Silva-Martinez, *Analog circuit design for process variation-resilient systems-on-a-chip*. Springer Science & Business Media, 2012.

[2] M. John. (2010, May) Dc output errors in a fully-differential amplifier. Application Note. Texas instruments. [Online]. Available: http://www.ti.com/lit/an/slva417/slva417.pdf

[3] D. Arbet, M. Kováč, L. Nagy, V. Stopjaková, and J. Brenkuš, "Low-voltage bulk-driven variable gain amplifier in 130 nm cmos technology," in *2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS)*, April 2016, pp. 1–6.

[4] D. Arbet, V. Stopjaková, M. Kováč, L. Nagy, M. Rakús, and M. Šovčík, "130 nm cmos bulk-driven variable gain amplifier for low-voltage applications," *Journal of Circuits, Systems and Computers*, vol. 26, no. 08, p. 1740003, 2017.

[5] B. James. (2011, April) Simple op amp measurements. Application Note. Analog Devices. [Online]. Available: http://www.analog.com/en/analog-dialogue/articles/simple-op-amp-measurements.html

[6] E. L. M. Ann, L. B. D. Howard, S. F. J. Emery, R. G. A. Davey, and R. R. R. James, "Development of device under test (dut) board of lm741 op-amp ic for test development and measurement track of mapua university," in *2017IEEE 9th International Conference on Humanoid, Nanotechnology, Information Technology, Communication and Control, Environment and Management (HNICEM)*, Dec 2017, pp. 1–4.

[7] *Recommended Test Procedures for Operational Amplifiers*, Application Note, Intersil, November 1996. [Online]. Available: https://www.intersil.com/content/dam/Intersil/documents/an55/an551.pdf

[8] P. Richard. (2001, March) Dc parameters: Input offset voltage (v_{IO}). Application Note. Texas instruments. [Online]. Available: http://www.ti.com/lit/an/sloa059/sloa059.pdf

[9] *Micropower, Zero Drift, True Rail-to-Rail Instrumentation Amplifier*, AD8237 Data Sheet, Analog Devices, 2012. [Online]. Available: http://www.analog.com/media/en/technical-documentation/data-sheets/AD8237.pdf