A Program Procedure for Estimation of the Cross–Coupled Charge Pump Properties

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Abstract—This paper presents the computional algorithm that is used for prediction of the cross-coupled charge pump static and dynamic properties. The calculation method is based on the state-space model of the charge pump for each phase of the clock signal. State equations are drawn from the symbolic relationships of the pump stage as an analog functional block using BSIM equations for long channel MOSFET. The algorithm was programmed in Maple SW and calculated values were compared with transistor-level circuit characteristics. The analysis results show high accuracy of the mentioned method, which allow to reflect many real effects compared to the equivalent digital model description. The algorithm will be used for synthesis procedure together with the application of formulae for optimal design circuit without long-time simulation process.

Keywords - BSIM model; Cross-coupled charge pump; cycle; recurrent expression; simulation; state-space model.

I. Introduction

Estimation of the static and dynamic properties of the cross-coupled charge pump (Fig. 1) through the mathematical description is a comprehensive task. Many reasons have been mentioned and demonstrated by the simulation results [5]. Simulations are the usual way of the optimal quasi-analog circuits design. Digital
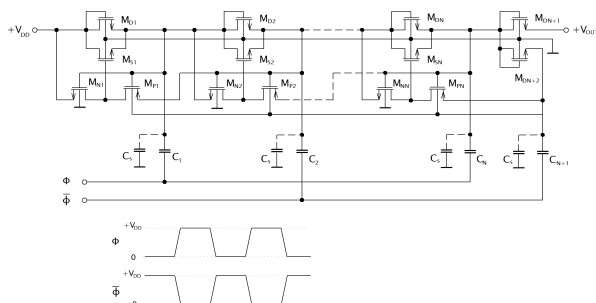

Fig. 1.   Cross-coupled charge pump [5].

model is not an option due to its low accuracy. However, another aproach has already been outlined in [5]. The previous research has been focused on the description of circuit behavior as an analog block. It allows to include many dominant and undesirable phenomenae (unlike the digital model description), which contribute

to reduce pump efficiency - reverse switch current, inverter cross current, body effect, etc. Complete model of each of the stages and last stage (Fig. 2) is detailed in [5]. Behavior of the model was tested in N-stages charge pump by the simulator LT SPICE. The analysis results show the match between the model and the full-transistor SPICE-level simulation in a wide set of the input parameters, as it was evidenced by the characteristics. Subtreshold region of MOSFETs is not expected in normal operation. Current research has
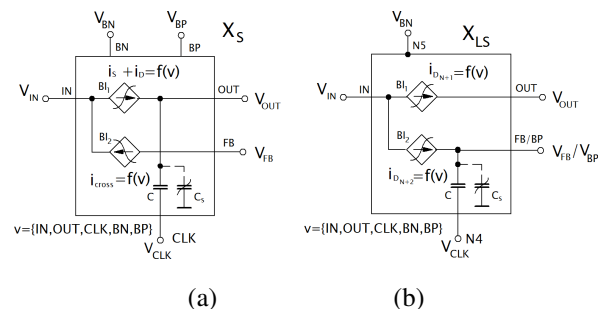

Fig. 2.   Subcircuit of the i-pump stage (a) and the last stage (b) [5]

built on the mentioned work. In this paper, the attention will be focused on the program procedure, which allow *to estimate the charge pump properties.* Firstly, the strategy of the solution through the state description of the system will be explained. The main part deals with principle of the computational algorithm which core is operating with previously derived analytic formulae of the analog blocks ([3], [6]). Algorithm is implemented in Maple SW and achieve results are compared with the full transistor-level properties of the charge pump, which are simulated in professional design environment ELDO. *The main benefit of our work is the development of step-by step synthesis procedure by using known relationships without the necessity to use computationally demanding iteration processes.*

II. State Model of the System

Generally, the classical control theory and methods that are used to simple input-output description of the plant can not be applied in this case. The reasons are
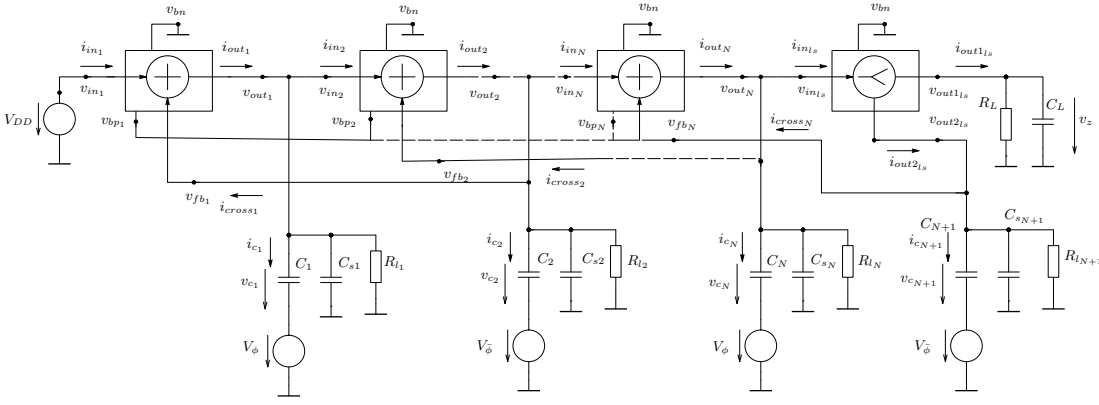
Fig. 3. Block diagram of the N-stage cross-coupled charge pump

based on the non-linear nature of the circuit, which handles discrete values–discontinuity of the inner states in time. But considering the selected time interval defined by the valid logic levels of the clock signals, the circuit may be described as *multidimensional continuous nonlinear dynamic system* [1]. The internal description leads to the state model of the system [2], block diagram is shown in Fig. 3. Each of the i-pump stage represents block, where the output current i_{out_i} is given by the sum of the input and cross inverter current, $i_{out_i} = i_{in_i} + i_{cross_i}$, and the block of the last stage splits the input current $i_{in_{ls}}$ into load current and charging current that flows through the last main capacitor C_{N+1}, then $i_{in_{ls}} = i_{out1_{ls}} + i_{out2_{ls}}$. The dynamics of the *state-space* system refers to *state variables represent by the voltage on the capacitors*, that fully describe the system at time $\langle 0, T_{clk}/2 \rangle$ and its response to any given set of inputs. Asuming the constant clock signal amplitude, the number of state variables with knowledge of those variables at initial time $t_0 \in \langle 0, T_{clk}/2 \rangle$ is equal to number of main capacitors because the time-varying component of the voltage v_{C_i} is the only one on the parasitic capacitor. In the other words $\dot{v}_{C_s} = \dot{v}_{C_i} + \dot{v}_{clk} = \dot{v}_{C_i}$ for valid logic levels. In the standard form, the mathematical description expressed as a set of N+2 (icluding load capacitance C_L) coupled first-order ordinary differential equations,

$$\dot{v}_{C_1} = \frac{1}{C_1 + C_{s_1}} \left[i_{in_1} - i_{in_2} + i_{cross_1} - \frac{v_{C_1} + V_{clk}}{R_{l_1}} \right]$$

$$\dot{v}_{C_2} = \frac{1}{C_2 + C_{s_2}} \left[i_{in_2} - i_{in_3} + i_{cross_2} - \frac{v_{C_2} + V_{clk}}{R_{l_2}} \right]$$

$$\vdots$$

$$\dot{v}_{C_i} = \frac{1}{C_i + C_{s_i}} \left[i_{in_i} - i_{in_{i+1}} + i_{cross_i} - \frac{v_{C_i} + V_{clk}}{R_{l_i}} \right]$$

$$\vdots$$

$$\dot{v}_{C_N} = \frac{1}{C_N + C_{s_N}} \left[i_{in_N} - i_{in_{ls}} + i_{cross_N} \right] -$$
$$- \frac{1}{C_N + C_{s_N}} \frac{v_{C_N} + V_{clk}}{R_{l_N}}$$

$$\dot{v}_{C_{N+1}} = \frac{1}{C_N + C_{s_{N+1}}} \left[i_{out2_{ls}} - i_{cross_N} \right] -$$
$$- \frac{1}{C_N + C_{s_{N+1}}} \frac{v_{C_{N+1}} + V_{clk}}{R_{l_{N+1}}}$$

$$\dot{v}_z = \frac{1}{C_L} \left[i_{out1_{ls}} - \frac{v_z}{R_L} \right] \qquad (1)$$

where $\dot{v} = \mathrm{d}v/\mathrm{d}t$. and each of the functions i_{in_i}, i_{cross_i}, $i_{out1_{ls}}$, $i_{out2_{ls}}$ is nonlinear time-varying function of the nodes voltages v_{C_i}, the system inputs (transistos sizing, power supply, etc.) and time. Resistors R_{l_i} model leakage current of each of the pump stages and R_L is main pump load resistance.

III. THE BASIC PRINCIPLE OF THE ALGORITHM

The state model is the core of the analysis algorithm despite its limitations that is mentioned in the previous text. The philosophy of the following approach that allow to estimate static a dynamic charge pump parameters is based on idea of the *quasi-analog system*. Block structure of the N-stage charge pump (Fig. 3), is described as analog circuit in each phase of the clock signal, while the transition into next phase is characterized by the discrete changes of some input variables (clock signal). The influence of the rising and falling edges of the clock signal is not considered. The new state is dependent on the new input variable but also on the previous state, i.e. recurrent expression. Algorithm diagram is shown in Fig. 4. Reffering to the input parameters (number of stages, clock frequency,...), program procedure automatically generates *state equations* from (1) with a set of initial conditions and sets amplitude of the clock signal V_ϕ, $V_{\bar{\phi}}$ from the number of cycle $k = \{1,2,...,n\}$,

$$V_\phi = \begin{cases} 0, & \text{for odd } k \\ V_{DD}, & \text{for even } k \end{cases}$$

Zero intial conditions are set in the first cycle that corresponds to the half of the period of the clock signal. It is very important point due to solution convergence. After initialization, the time response characteristics $v_{C_i}(t)$ and $v_z(t)$ are computed at time interval

$$t \in \left\langle (k-1)\frac{T_{clk}}{2}, k\frac{T_{clk}}{2} \right\rangle.$$

The end value of the interval is passed as the parameter determining the initial condition to the next cycle. In general form, the inital condition of each of the state
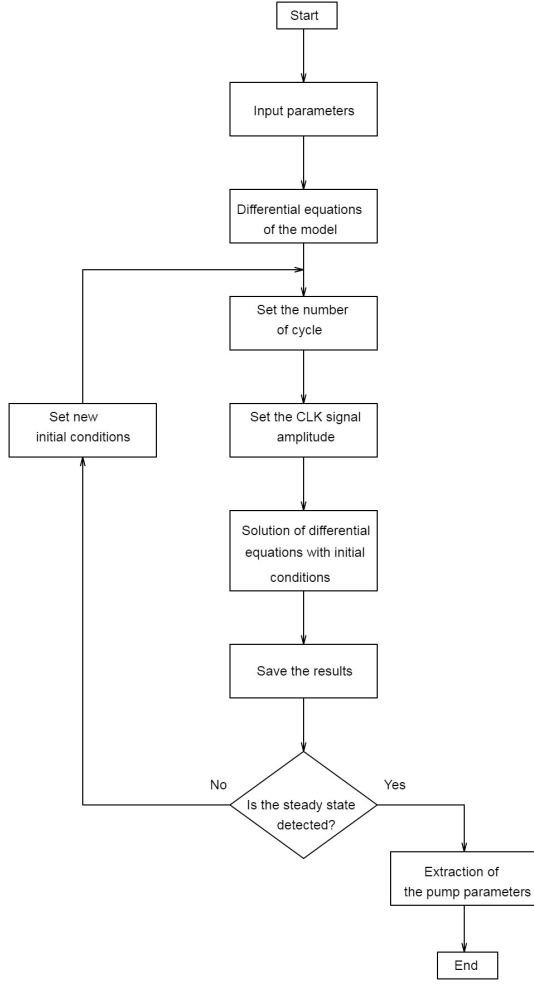
Fig. 4. Charge pump analysis algorithm

Fig. 5. Time response characteristics of the pump output voltage

variables, labeled $v_{C_{i_0}}^{(k+1)}, v_{z_0}^{(k+1)}$, in the next cycle is determined as

$$v_{C_{i_0}}^{(k+1)} = \text{sgn}_{V_{DD}} V_{DD} \cdot \frac{C_s}{C + C_s} + v_{C_i}^{(k)}|_{t=k \cdot T_{clk}/2},$$

$$v_{z_0}^{(k+1)} = v_z^{(k)}|_{t=k \cdot T_{clk}/2},$$

$$\text{for } t \in \left\langle k\frac{T_{clk}}{2}, (k+1)\frac{T_{clk}}{2} \right\rangle, \quad (2)$$

where factor $\text{sgn}_{V_{DD}}$ provides sign of the clock signal amplitude:

$$\text{sgn}_{V_{DD}} = \begin{cases} +1, & \text{for the passive interval of CLK} \\ -1, & \text{for the active interval of CLK}, \end{cases}$$

after that, the computing process is repeated.

As a result, dynamic behavior of the system within the interval $t \in \langle 0, k \cdot T_{clk}/2 \rangle$ is obtained by composing partial response characteristics in the appropriate scale.

Computional procedure runs until the the output voltage $v_z(t)$ achieves the steady state. It means that average value of the output voltage is practically constant over time.

Steady state is simply indicated by comparing two arbitrary values that are temporarily shifted by just one period of the clock signal (see Fig. 5). Consequently,

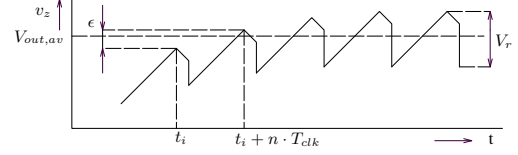$$v_z(t_i + T_{clk}) - v_z(t_i) < \epsilon, \quad (3)$$

where parameter ϵ should be chosen with regard to the numerical calculation accuracy, for example $\epsilon = 1\,\text{mV}$.

IV. EXPERIMENTAL PART

The computational algorithm has been programmed in Maple SW according to the structure that is shown in Fig. 3. The influence of the parasitic capacitances C_{s_i} and shunt resistances R_{l_i} is taken into account. All the simulations parameters are given in Tab. I.

Under condition (3), the values of the system state variables can be used used to calculate other significant parameters, as power consumption, etc. In addition, procedure checks correct function of the circuit (open loop of feedback is a typical problem for this topology), operation mode of each of the transistors and exceeding the limit parameters ($V_{DS_{max}}$, $V_{GS_{max}}$, etc.).

Total number of cycles, labeled n, when the output voltage v_z starts from the initial value to the final value in steady state is approximately equal to *Rise time* T_r,

$$T_r \approx \frac{n}{2} T_{clk}|_{k=n}. \quad (4)$$

The voltage trend over time $v_z(t)$ is actually difficult to describe, because it is influenced by many dynamic effects in circuit, as capacitive couplings between stages and charge injection. An example of time response characteristic is shown in the Fig. 6.

Average value $V_{out,av}$ of the output voltage is estimated as the average value of the minimum and maximum values instead of the numerical integration of $v_z(t)$ in steady state,

$$V_{out,av} \doteq \frac{v|_{t=k \cdot T_{clk}/2} + v|_{t=(k+1) \cdot T_{clk}/2}}{2}, \quad (5)$$

where k is close to n. The output ripple voltage, labeled V_r, is given by the difference of the maximal and minimal values,

$$V_r = |v_i - v_{ii}| \text{ for } k \to n, \quad (6)$$

where $v_i = v|_{t=k \cdot T_{clk}/2}$ and $v_{ii} = v|_{t=(k+1) \cdot T_{clk}/2}$.

Static and dynamic characteristics were compared with values that have been analyzed by the professional simulator ELDO including SPICE-level models of the components (library MGC Design Kit). Some results are summarized in the following table, including relative average output voltage error $\epsilon_{V_{out}}$. Naturally, the computional time increases with the number of circuit nodes, which is associated with the number of pump stages. However, total cycle count is a crucial indicator of computational difficulty. The growth trend, as it is shown in Fig. 7, is limited by the *pump efficiency*.
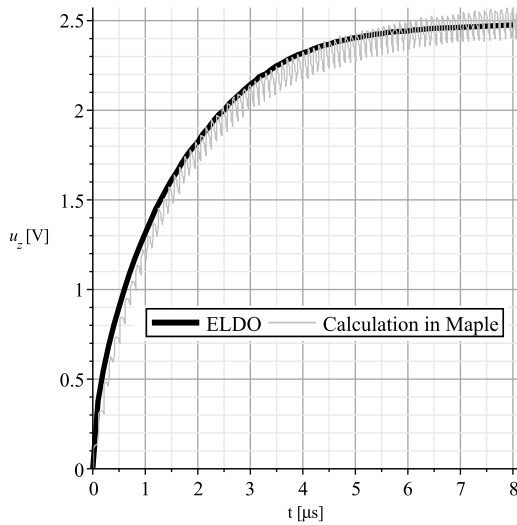
Fig. 6. Time response characteristic of the five-stage pump output voltage

V. CONCLUSION

The analysis algorithm for estimation of static and dynamic parameters of the cross-coupled charge pump was discussed in this paper. The principle is based on the state model analyzing circuit behavior at each phase of the clock signal. The block structure was built from the subcircuits, which include dominant effects via the BSIM model equations. N-stage charge pump structure is described by the N+2 first-order differential equations. Total response characteristics of the output voltage is obtained through the composition of partial responses for each phase of CLK with initial conditions. Algorithm was implemented in Maple

software and calculated parameters were verified by the simulations in the professional design software ELDO, Design Architect-IC v2008.2_16.4 including the SPICE-level component models in library MGC Design Kit. This method is very accurate because the
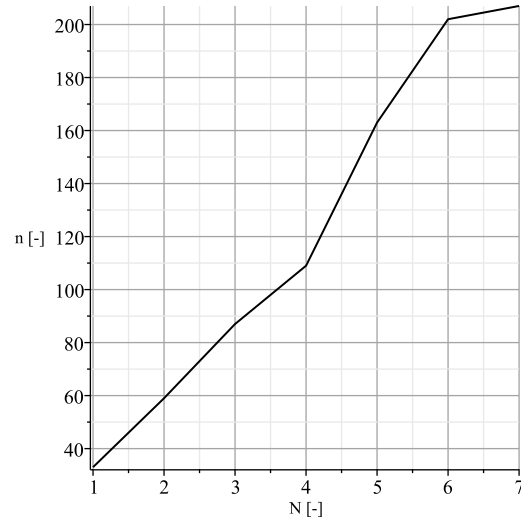

Fig. 7. Number of cycles vs number of stages

transistor-level properties can be arbitrarily included in the sub-blocks description, unlike the "digital circuit perception". Furthermore, the knowledge of the state variables allows to estimate many other parameters, for example, power efficiency. On the contrary, the disadvantage is the need to use a recurrent description associated with the total number of cycles. Computational difficulty is derived from the complexity of circuit topology and pumping efficiency (voltage increase) in time, see Fig. 7.

The main benefit is using the algorithm for synthesis procedure. Future work involves Ward´s capacitance model into the structure, next step is creation of the design algorithm that is using the existing relationships.

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