# Current Limiting Driver for GaN Half-Bridge

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***Abstract* – This paper presents a GaN transistor half-bridge prototype with robust pulse by pulse current limiting drivers designed to turn off safely the transistor for the rest of the PWM period when the drain current exceeds the set value. The half-bridge is intended as the key part of a DC/AC converter output stage with operating frequency up to 1 MHz. The current limiting circuit is designed to meet the requirements for safe operation of GaN transistors. The proposed current limiting driver is five times faster compared to common integrated drivers with included current limiting circuit.**

***Keywords – GaN MOSFET; half-bridge; driver; current protection.***

## I. INTRODUCTION

The fast developing technology of Gallium Nitride (GaN) power MOSFET transistors is calling for a new sophisticated high speed driver. The fact of GaN transistor no reverse recovery charge allows us to design a new level of high frequency DC/AC converters with high efficiency and power density.

The goal of the driver is to operate the transistor within the whole range of its parameters. High speed current limiting driver was described in [1] for Silicon Carbide (SiC) transistors but GaN transistor has the potential to operate on higher frequencies and therefore the driver must be fast enough.

For most of converter types, the main benefit of the increased operating frequency is increasing the power density. The higher frequency is reached, the smaller inductance is needed. Thereafter the cores can be smaller and, number of turns lower, which means that the conductivity losses in copper are substantially reduced and the efficiency significantly increases.

For off-grid operating DC/AC converters the output short circuit or time limited overload is common and the converter has to handle it without troubles. These high efficiency converters provide very low output resistance compared to the grid which causes short-circuit currents much larger. The driver has to be able to turn off the transistor safely when the drain current nominal or desired value is exceeded.

## II. GALLIUM NITRIDE BASIS

### A. No Reverse Recovery

GaN transistor does not contain substrate free-wheeling diode compared to Si or SiC MOSFETs. Nevertheless, GaN transistor allows reverse conduction without reverse recovery charge.

In reverse conduction region the positive gate voltage must be applied to reach low on-resistance. When looking into datasheets of today's available GaN, for example [5], the on resistance in reverse conduction can supply the freewheeling diode not with bigger conduction losses compared for example to IGBT.

### B. Output Capacitance Linearity

Unlike Si or SiC, GaN structure offers linear change of the output capacitance during turning-off, see [2].

The main benefit of output capacitance linearity is represented by the constant di/dt slew rate during turning-on and turning-off. Stable slew rate is important at higher frequencies when especially the whole converter mechanical design limits the maximum di/dt capability.

### C. Gate Driving Requirements

The GaN transistor has approximately 10 times lower gate charge compared to Si MOSFET of the same power category, see [4].

More important is to choose a driver operable at the desired frequency. Propagation delays of the driver output stage are now important because they cause PWM signal distortion when on and off delays are not equal.

In datasheets some MOSFET drivers are labelled as ultrafast, for example see [6], but unfortunately nowadays they are still too slow for GaN transistor and the driver output stage is what limits the maximum PWM frequency.

## III. GAN DRIVER ON REFLECTION

### A. Current Measuring

The method of measuring the drain to source voltage when transistor is turned on had been chosen to determine the current. The drain on-resistance is stable defined value in the datasheet so it can be used for calculation of the maximum voltage allowed across the drain-source channel.

The calculated value is then set as a reference for fast comparator that is measuring the voltage to determine the maximum current allowed.

The pulse by pulse current limiting consists of RS flip-flop, so the transistor remains turned off until the next rising edge of the input signal is received. However, it depends on the controller that receives the

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error signal when the next rising edge to turn on will come.

The output stage of the driver is equipped with a high speed tri-state IC driver what enables input driven according to the TABLE I.

TABLE I. GATE CONTROL LOGIC

| Input Signals | | Output |
|---|---|---|
| PWM Input | Fault | Gate |
| 0 | X | Off |
| Rising edge | 0 | On |
| 1 | Rising edge | Slow turn off |

### B. *Safe Turn-off Over-current*

The bigger is the current the higher is the di/dt when turns off since the fall time does not change. High di/dt is causing overvoltage. To prevent the damage of the transistor during the turning off over-current the gate is discharged through the extra path with higher resistance compared to normal turn-off. Higher gate turn off resistance is discharging the gate slower which causes the transistor to turn off slower, too.

Figure 1. compares the desired turn off with that one caused by the driver delay.

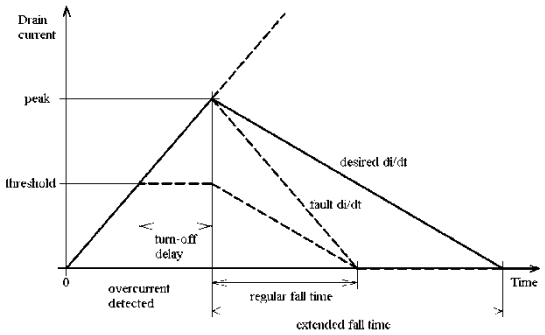
The threshold current is set to reasonable value but the peak current will be higher due to the propagation delay of the driver.

Compared to Si IGBT and SiC where this method is also used [1], the delay of driver itself is significant. GaN is much faster, even compared to today's IC drivers, and the delay since the over-current detection till the actual start of turning off has to be considered.

### C. *PCB Desing*

The path that contains low side transistor, high side transistor, and dc-link capacitor has to be designed with the lowest possible parasitic inductance.

Figure 1. Fall time extending.




Parasitic inductance causes voltage peaks during the transistor turning-off in this path. There are some methods how to decrease this phenomenon.

Basic one is to connect the path using short but wide copper islands instead of thin and long ones. Multiple layer board allows cancel most of the inductance when routing the path in the next layer to the opposite direction making it a choke with really small square area. This leads to the need of placing dc-link capacitors in-line with the half-bridge transistors [3].

## IV. DESIGNED PROTOTYPE

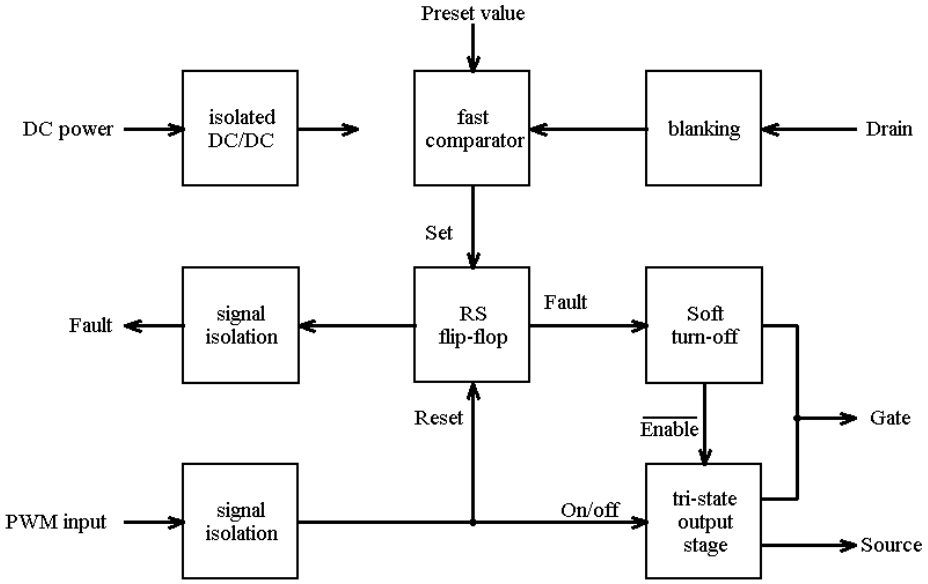
Based on the driver reflection a prototype had been designed.

### A. *Block Schematic*

In Figure 2. one side of the half-bridge driver is described.

The isolation barrier is equipped with bidirectional isolators for input PWM signal and fault output. The DC/DC converter provides power for the logic and the output stage of the driver, too. Both low and high sides have their own isolators and DC/DC isolated converters.

Figure 2. Block diagram of the current limiting driver.



The PWM signal feeds directly the IC output stage which is tri-state buffer that controls the gate in normal operation.

Current is measured using voltage across the transistor on-resistance which is stable enough across the temperature range according the datasheet [5]. Sampling circuit is necessary to measure it only when turned on and respects the delay of the signal path so that the comparator doesn't receive false voltage before the transistor starts to turn-on.

Fast comparator has preset value of maximum drain to source voltage and when the measured value is higher the output fault signal is set.

Fault signal changes the state of the RS flip-flop in the way that the output stage is forced to high impedance and gate is discharged through a path with higher gate resistance to achieve the over-current soft turn off.

### *B. Testing the Prototype*

The designed prototype half-bridge is shown in Figure 3. For testing the over-current protection one more board with high-side GaN only and SiC Schottky diode in the low-side was made. The over-current protection was then tested according to simplified circuit scheme drawn in Figure 4.

Measured delay times are presented in Table II. and in Figure 5. Measured values are compared with values of another driver equipped with similar over-current protection ACPL339J. The used ACPL339J values are taken over from [1].

Figure 3. PCB prototype.

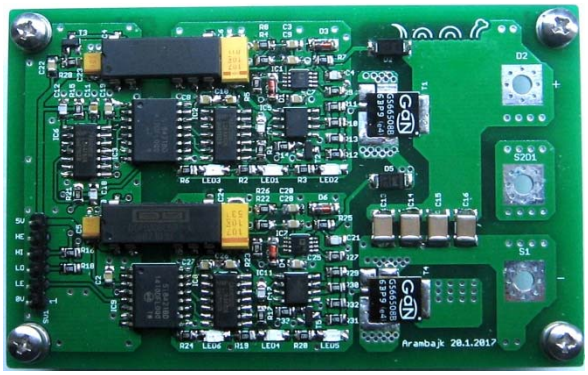


Figure 4. Simplified circuit for testing the over-current protection reaction on short circuiting of the converter output.

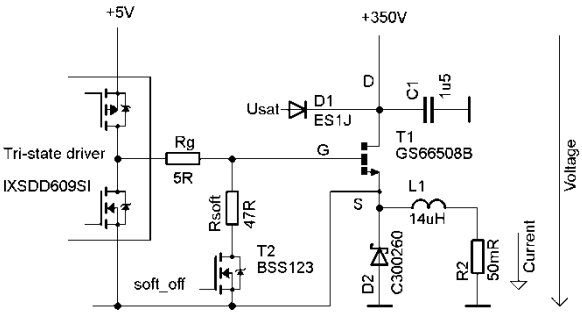
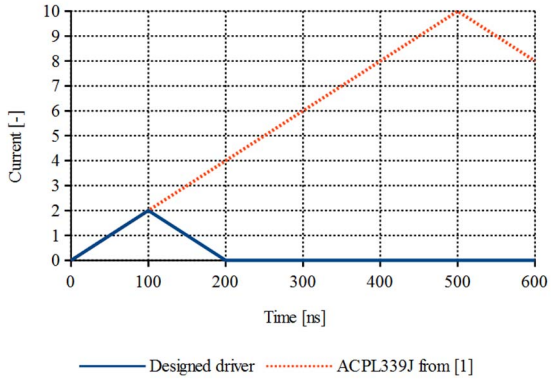



TABLE II. CURRENT PROTECTION RESPONSE TIME

| | Time [ns] | |
|---|---|---|
| | ACPL339J from [1] | Designed driver |
| Blanking | 200 | 50 |
| Turn-off delay | 300 | 50 |
| Turn-off fall | 300 | 100 |
| Total | 800 | 200 |
| Respond time | 500 | 100 |

Figure 5. Comparison of the current protection response times reckoned with relative current values assuming both drivers used in the same circuit shown in Figure 4. The ACPL339J graph is drawn on base of the data given in [1].

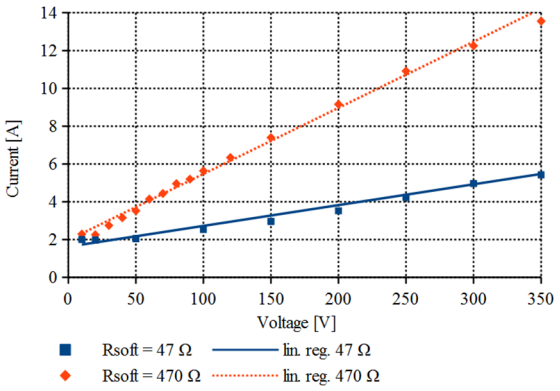



Response times were measured with two different $R_{soft}$ resistors of 47 Ω and 470 Ω which means 10 times and 100 times higher resistance than that of the regular turn-off resistor $R_g$.

Higher resistor value prolongs the turn-off delay since the voltage has to drop below the gate threshold. Simple clamp circuit from [1] will improve it.

Measured results are shown in Figure 6. and in **Error! Reference source not found.**as a peak current and converter on-time depending on the applied voltage. The inductance remains the same which means that different voltage gives different di/dt for each point.

Figure 6. Peak current depending on voltage and $R_{soft}$.




Resistor $R_{soft}$ needs to be set for the designed circuit not to prolong the on-time too much, but on the other hand to allow soft turn-off to prevent overvoltage.

The Figure 7. shows how the over-current protection works with inductive load. On Figure 8. it is shown the delay between over-current detection and the transistor turn-off. Figure 9. shows the slow gate discharge that occurs when the over-current protection was tripped. The protection was set to 3 A.

Figure 7. Inductive load turn-off with the over-current protection set to 3 A, yellow is current as 50mV/A and blue is voltage across the load according to the Figure 4.

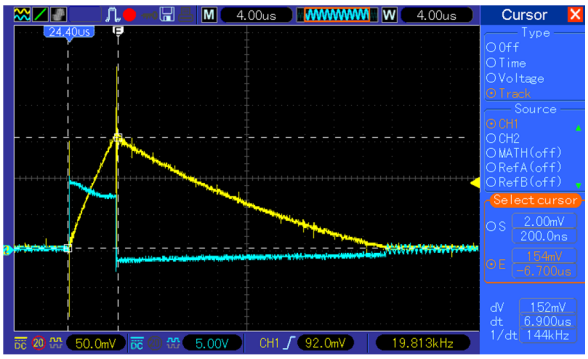



Figure 8. Over current detection turn-off delay. Blue line is the output of a comparator that detects the over current and the yellow is voltage across the load (measured at different voltage than previous picture.)

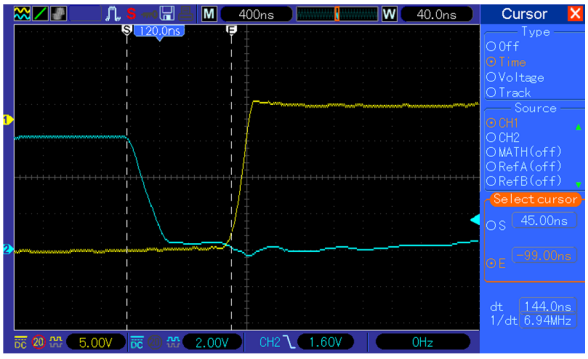
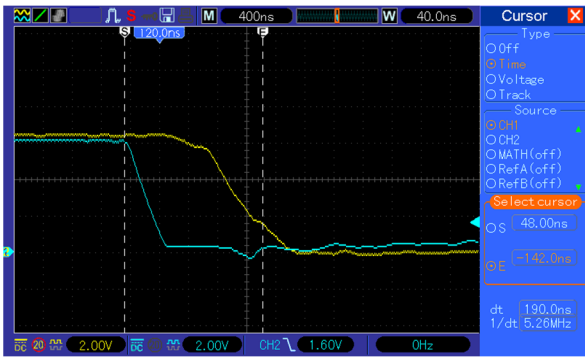



Figure 9. Slow gate discharge after over-current detected. T|he yellow is voltage at the gate and blue comparator output to show when the over-current was detected.




## V. Conclusion

The designed GaN transistor half-bridge has been tested to meet successfully the desired operation frequency of 1 MHz and to achieve properly turn-off with current limiting driver at converter output short-circuiting to ensure the transistor operation within its entire range and to exploit fully its limits.

The results obtained are showing that the driver output stage limits the maximum switching frequency when using standard integrated drivers. The driver propagation delay has to be considered when using GaN transistors to fabricate power converters working at high frequencies.

To increase the maximum operating frequency a faster driver output stage needs to be built up.

Next step will cover adding voltage measurement during turning-off and fast signal processing to control the whole safe operating area and to make possible to use the driver with multiple types of transistors without driver circuit changes.

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