Groups of Synchronizers for Communications by Fiber Optic

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***Abstract*- This work studies a digital transmission system by fiber optic. We give special relevance to the synchronism block. The fiber is a transmission medium with large bandwidth and low attenuation. These characteristics allow high speed and long distances. The transmission, instead asynchronous, it is synchronous what provides a big efficiency of 100%. However, the synchronous transmission needs a synchronizer. The objective is to study the synchronizers and their performance of output jitter Unit Interval Root Mean Square (UIRMS) versus input Signal Noise Ratio (SNR).**
Keywords **– Optical Digital Transmission, Synchronism**

I. INTRODUCTION

This work presents a synchronous digital system, where the transmission channel is the fiber optic.
The fiber optic has wavelengths windows λ of very low attenuation (1st in 850nm with attenuation 2dB/km, 2nd in 1310nm with attenuation 0.5dB/km and 3rd in 1550nm with attenuation 0.25dB/km). Fig.1 shows the fiber optic cable and their transmission windows.

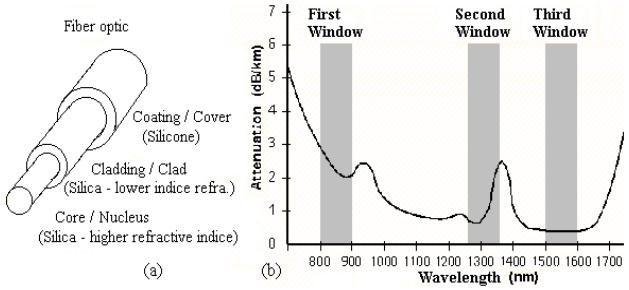

Fig.1 Fiber optic (a) and their three transmission windows (b)

The fiber has low attenuation, what allows the signal to reach great distances without repeaters. Its bandwidth is very large (1000 times greater than cooper cable), what provides high speed and high information density [1 - 10]. One fiber is able to transport multiservices, such as sound, image and data. The fiber is constituted essentially by silica that exists in great abundance in the nature. However, the cooper reserves are diminished considerably. The optical signals have different nature, therefore they have great immunity to electrical interferences.
The transmission can be synchronous or asynchronous, the last has better efficiency (100%), since there is no start neither stop bits and all bits are information. However, the synchronous communication requires the synchronizer block (clock recover), which is here studied in special.
In past and actual state of the art were developed various synchronizers, but now we wish to measure their quality.

The motivation of this work is to create new synchronizers and to study their performance with noise. This contribution improves the knowledge about synchronizers.
Firstly, we present the general system. After, we present the synchronizer task. After, we present the synchronizer composition. After, we present two synchronizer groups. Then, we present the project and tests. After, we present the results. Finally, we present the conclusions.

II. GENERAL SYSTEM DESCRIPTION

Fig.2 shows the digital transmission system by fiber optic, with various blocks, highlighting the synchronizer block.

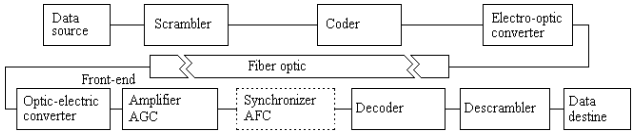

Fig.2 Communication system by fiber optic with the synchronizer

In emitter, the block data source supply the data, the scrambler equalizes the spectrum ignoring the input, the coder guarantees a constant DC component and transitions, the electric - optic converts the electric signal into light to pass through the fiber.
In receiver, the front- end (optic- electric and pre- amplifier with Automatic Gain Control- AGC) transforms newly the optic signal into electric with constant amplitude, the synchronizer with Automatic Frequency Control (AFC) recovers the clock and samples and retimes the data, the decoder makes the inverse of coder, the descrambler makes the inverse of scrambler and the data destine is the final.

III. THE SYNCHRONIZER TASK

We highlight the synchronizer, which extracts the clock to make two essential functions. The 1st is to sample the data in the maximum eye diagram to minimize the error rate, the 2nd is to retime the data to the bit original duration [1, 2]. Fig.3 illustrates these two basic functions.

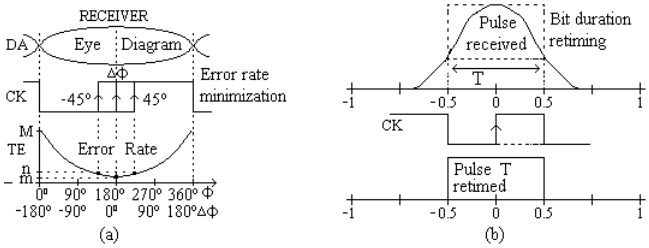

Fig.3 Data sampling (a) and data retiming (b)

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In a digital system, normally, the clock is also available to be utilized by other blocks.

IV. THE SYNCHRONIZER CONSTITUTION

The synchronizer, normally, consists of three essential blocks which are: input adapter, clock recover and output decision [3, 4]. Fig.4 shows the synchronizer aspect.

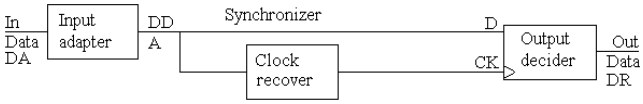

Fig.4 Synchronizer blocks: adapter, recover and decision

The adapter formats the input data, the recover recoveries the clock and the decision decides correctly de output data.

V. OPERATION MODE OF SOME SYNCHRONIZERS

There are many types of synchronizers. Each one has its operation mode. We consider three classes which are the open loop, mixed loop and closed loop. In the closed loop, we consider four types which are the analog, hybrid, combinational and sequential. In the sequential, we present the reference pulse comparison group developed by Hooge [3] and the new proposed group developed by us [9]. Fig.5 illustrates respectively their operation mode (Fig. 5).

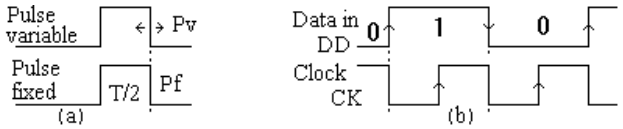

Fig.5 Base of the pulse comparison (a) and clock sampling (b)

The 1st group is based in the comparison between a variable pulse Pv (variable clock phase) and a fixed pulse Pf (fixed clock phase at bit center)(a). The 2nd group is based in the sampling of the clock by the data transitions (b).

VI. GROUPS OF COMPARISON AND SAMPLING

We show two sequential synchronizers, one is based on a pulse comparison and the other on a clock sampling.

A. Group based on pulse comparison

The reference group, proposed by Hooge, is based in the comparison between a variable pulse Pv (varable clock phase) and a fixed pulse Pf (fixed clock phase at bit center). Pv is the time between data transition and clock positive transition and Pf is the time between two clock transitions.
The variable pulse Pv varies between 0-T and the fixed pulse Pf is half period T/2 [4].
According to this comparison, we consider two versions, which are the manual and the automatic. The variable pulse Pv is common to the two versions, but the fixed pulse Pf is different in each version.
Fig.6 shows the manual version.

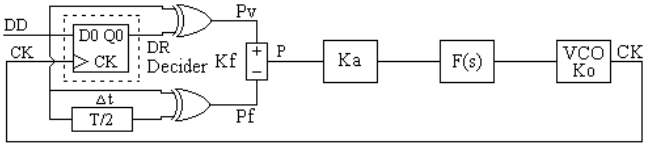

Fig.6 Group of pulse comparison and manual version (PCm)

In this version, the fixed pulse is produced by the delay line T/2 pre adjusted manually with the 2nd exor.
Fig.7 shows the automatic version.

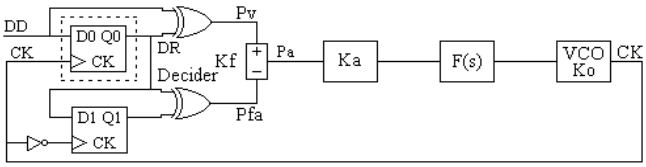

Fig.7 Group of pulse comparison and automatic version (PCa)

In this version, the fixed pulse is produced automatically by the 2nd flip flop with the 2nd exor. This pulse don't needs any human pre adjustment.

B. Group based on clock sampling

The proposed group by us, is based in the sampling of the clock by the data. Then, if necessary, the error pulse Pe, corrects the clock along the bit 0-T. At the equilibrium, the clock is at the bit center T/2, the error pulse average Pe is null and the clock position is maintained [9].
According to the error pulse creation Pe, we consider two versions which are the manual (CSm) and automatic (CSa). In both versions, the flip flop FF0 samples the clock position. The difference is in the pulse Pe, it can be generated by a manual pre adjustable delay line or automatically by a flip flop. This adjustment is not critical.
Fig.8 shows the manual version

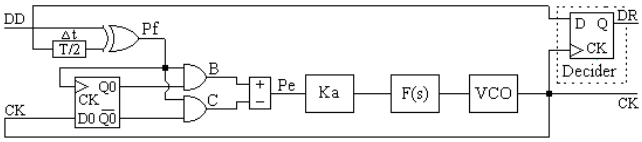

Fig.8 Group of clock sampling and manual version (Csm)

Here, the load fixed pulse Pf=T/2 is generated by the delay line pre adjusted manually with the exor. This pulse is produced without help of the clock. Fig.9 shows the automatic version

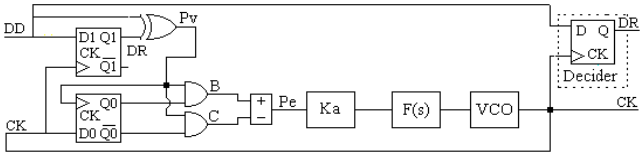

Fig.9 Group of clock sampling and automatic version (CSa)

Here, the load variable pulse Pv is produced automatically by the flip flop FF1 with exor. At equilibrium, Pv tends to T/2 and is in phase with the data.

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VII. PROJECT, TESTS AND RESULTS

We will present the project, tests and results of the designated synchronizers [5].

A. Project

All the synchronizers were projected with the same linearized transfer function, guarantying the same test conditions.

The loop gain is Kl=Kd.Ko=Ka.Kf.Ko, where Kf is the phase detector gain, Kd is the phase comparator gain, Ko is the VCO gain, F(s) is the loop filter and Ka is the control that acts in the root locus providing the desired characteristics.

To facilitate the analyze, we used a normalized bit rate tx=1baud, what implies normalized values for the other parameters. So, we used a normalized clock frequency fCK=1Hz, a normalized external noise bandwidth Bn=5Hz and a normalized loop noise bandwidth Bl = 0.02Hz. After, we desnormalize this values to the correspondent ones.

The signal power is $Ps=Aef^2$ and the noise power is Pn = No.Bn. The noise spectral density is $No=2\sigma n^2.\Delta\tau$, where $\Delta\tau=1/fSamp$ is the sampling period and σn^2 is the variance.

The relation between the SNR and the noise variance σn^2 is $SNR=Ps/Pn=A^2_{ef}/(2\sigma n^2.\Delta\tau.Bn)=0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2$.

After, we will obtain the jitter UI as function of the SNR. The loop dimension is

- 1st order loop:

The loop filter F(s)=1, with cutoff frequency 0.5Hz (Bp=0.5Hz is 25 times Bl=0.02Hz), eliminates only the high frequencies, but maintains the loop characteristics.

The transference function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (1)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (2)$$

So, for the analog synchronizer (Km=1, A=1/2, B=1/2; Ko=2π) the loop noise bandwidth is *Bl=0.02=(Ka.Kf.Ko)/4, then*

$$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2/\pi \quad (3)$$

For the hybrid synchronizer (Km=1, A=1/2, B=0.45; Ko=2π), the loop noise bandwidth is *Bl=0.02=(Ka.Kf.Ko)/4*, then

$$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2.2/\pi \quad (4)$$

For the combinational synchronizer (Kf=1/π; Ko=2π), the loop noise bandwidth is *Bl=0.02=(Ka.Kf.Ko)/4*, then

$$(Ka*1/\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.04 \quad (5)$$

For the sequential synchronizer (Kf=1/2π; Ko=2π), the loop noise bandwidth is *Bl=0.02=(Ka.Kf.Ko)/4*, then

$$(Ka*1/2\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.08 \quad (6)$$

The jitter depends on the effective signal Aef, noise spectral density No and loop noise bandwidth Bl.

For the analog PLL, the jitter formula is

$\sigma\phi^2=Bl.No/Aef^2=Bl.2.\sigma n^2.\Delta\tau=0.02*10^{-3}*2\sigma n^2/0.5^2=16*10^{-5}.\sigma n^2$

For others PLLs the jitter formula is more complex.

- 2nd order loop:

The 2nd order loop is not projected here, but the results are similar.

B. Tests

We used the following setup, to obtain the jitter- noise curves of the various synchronizers (Fig.10).

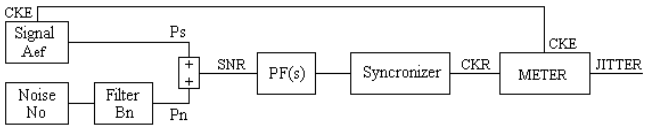

Fig.10 Blocks diagram of the test setup

The signal with noise gives a receiver recovered clock with jitter that is compared with the original emitter clock without jitter, the difference will be the jitter of the recovered clock.

C. Jiiter measurer (Measurer)

The jitter measurer consists of the flip flop RS that detects the variable phase of the recovered clock (CKr), relatively to the fixed phase of the emitter clock (CKe). This relative random variable phase is the recovered clock jitter (Fig.11).

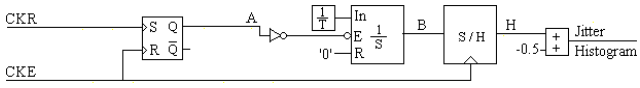

Fig.11 Jitter measurer (Measurer)

The other following blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram, see waveforms of Fig.12.

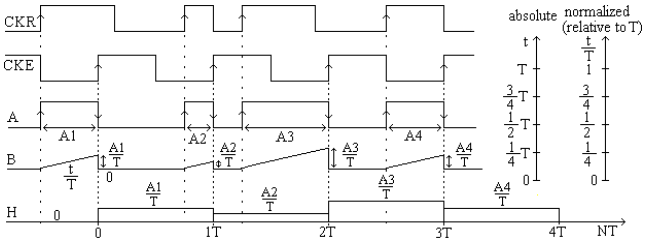

Fig.12 Waveforms of the jitter measurer (Measurer)

Then, the jitter histogram is sampled and processed by an appropriated program, supplying the jitter UI-RMS and the jitter pick to pick UI-PP.

D. Results

We present the results in terms of output jitter UI-RMS versus input signal noise ratio SNR. Fig.13 shows the jitter-SNR curves for the group pulse comparison with versions manual and automatic (PCm, PCa) and for the group clock sampling with versions manual and automatic (CSm, CSa).

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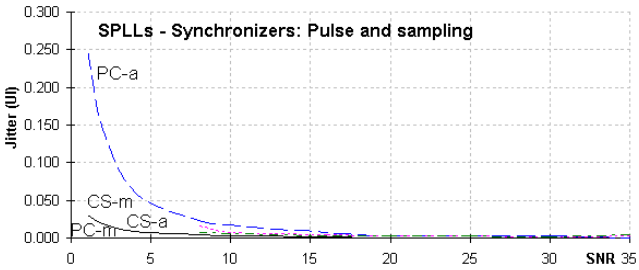

Fig.13Jitter-SNR curves of the 4 synchronizers(PCm,PCa,CSm,CSa)

We verify, that generally, the output jitter diminishes gradually with the input SNR increasing.

For high SNR, the four synchronizers have similar behavior. For low SNR, the pulse comparison manual is significantly the best, in follow are the clock sampling versions and the pulse comparison automatic is slightly the worst.

The group pulse comparison has synchronism difficulty for SNR < 4 and the clock sampling for SNR < 8.

VIII. CONCLUSIONS

This work studied two groups of sequential synchronizers, namely the pulse comparison with versions manual (PCm) and automatic (Pca) and the clock sampling with versions manual (CSm) and automatic (CSa). We noted that the output jitter decreases gradually when the input SNR increases.

For high SNR, the 4 synchronizers have similar jitter, since all them are digital and then with the same noise margin.

For low SNR, the PCm is significantly the best, the clock sampling versions (CSm, CSa) are the intermedium and the PCa is slightly the worst. This is comprehensible since PCm has only one memory error state (1 flip flop) contributing to the jitter and the error pulse disappear at equilibrium. The CSm and CSa have also one state but the error pulse don't disappear at equilibrium. The PCa has two error states (2 flip flop) contributing to the jitter and the error pulse exists with null average.

The clock sampling, relatively to the pulse comparison, don't needs critical adjustments.

The pulse comparison begins with synchronism problems for SNR < 4 and the clock sampling for SNR <8.

In practice, the group pulse comparison has adjustments more critical than the clock sampling.

In the future, we are planning to study other types of synchronizers.

ACKNOWLEDGMENTS

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