A Carrier Redistribution PWM for Dual Inverter with Separated DC Circuits

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***Abstract*—This paper deals with a proposal of a carrier redistribution PWM and its comparison with a phase disposition PWM (PDPWM) and carrier redistribution PWM for a multilevel converter dedicated to high power medium voltage electric drives. The converter topology is based on a cascaded connection of two-level inverters, the so called dual inverter. The well known phase disposition PWM for multilevel converters is modified for the above mentioned topology and its derivation as carrier redistribution PWM (CRPWM) strategy is employed. The proposed CRPWM enables the reduction of unbalanced load of the power electronics switches and increasing in the maximum output power rate. The functionality of the proposed PWM strategy has been verified on a simulation model of the converter as well as by experiments. The proposed PWM strategy has been compared with the standard PDPWM according to selected criteria such as total power losses, balanced load of switching devices and THD of phase load voltage waveforms.**

***Index Terms*—Multilevel converter, dual inverter, carrier redistribution, phase disposition, PWM, power losses, THD.**

INTRODUCTION

As the demands of industry applications on power electronics have increased in last decades, the multilevel converter (MLC) topologies became popular. In multilevel configurations, the dc voltage is divided among a number of components, therefore the voltage stress on power semiconductors is lower, the output voltage steps during switching is lower and the amplitudes of harmonics in side band are reduced [1].

There are many known topologies of multilevel converters. The best known typical configurations are neutral point clamped converters (NPC), flying capacitors converters (FLC), cascaded H-bridges (CHB), modular multilevel converters (M2LC) [2], [3], [4]. Each of the mentioned configurations has different advantages. The advantage of the M2LC is a simple process of scaling output voltage levels by linear addition of identical modules. However, the conduction losses of the M2LC are increased by a circulating current caused by unbalanced capacitor voltages. Moreover, the capacitor voltage ripple depends on the output frequency and it is higher for the lower output frequencies.

NPC, FLC and CHB do not have any circulating currents, however in the FLC and NPC respectively the additional number of elements is required. The advantage of the FLC and the CHB over the NPC is the number of redundant switching combinations which allow a dc circuit voltage balancing [5]. Moreover, the CHB does not have any additional capacitors or diodes. However, the main drawback of the CHB is requirement of separated dc circuit per each cell [6]. A simple modular solution to decrease the number of dc circuits can be a multilevel converter represented by the so called dual two-level inverter connection with separated dc sources with equivalent dc sources the dc voltage balancing is not an issue [7].

These topologies could be controlled by several modifications of pulse width modulation known as phase shifted PWM (PSPWM), phase disposition PWM (PDPWM) and space vector PWM [8], [9], [10]. Previous research has demonstrated that the average transistor switching frequency of PDPWM is lower than the average transistor switching frequency of PSPWM. However, the disadvantage of the PDPWM is an unbalanced load of IGBTs [11]. Using the PDPWM, the unbalanced voltage in the dc circuit can appear, and this leads to higher voltage stress on switching elements and the shorter lifetime of capacitors [12]. Therefore, several modifications of PDPWM techniques, such as the selective loop bias mapping PDPWM (SLBM-PDPWM), the carrier redistribution PWM and the multiple carrier modulation with dc stack current injection modulation have been developed and presented in [13], [14], [15]. These methods are able to reduce the unbalance of capacitor voltages for several MLC topologies including FLC, NPC, CHB. As shown in chapter , some of these modifications can be used to achieve balanced load of IGBTs and to increase the maximum output power rate of the dual level inverter with equal separated dc sources.

The goal of this paper is to propose a CRPWM based control for the dual inverter and to verify that the proposed CRPWM has the balanced load of semiconductor switches (IGBTs). The paper also seeks to compare this control method with the PDPWM for the dual inverter with separated dc link multilevel topology.

DUAL INVERTER TOPOLOGY

The topology of the multilevel converter based on a dual inverter topology is shown in Fig. 1. This topology requires lower number of dc voltage sources (dc capacitors) and does not have any clamped diode or capacitors. Furthermore, the dual inverter does not need to be connected to the middle of dc link capacitors,

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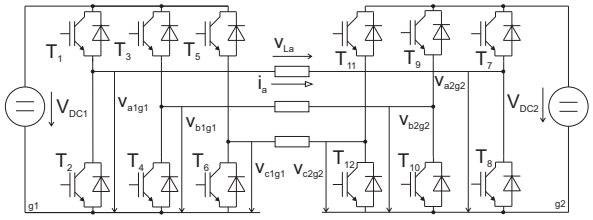

Figure 1. Topology of dual two-level inverter.

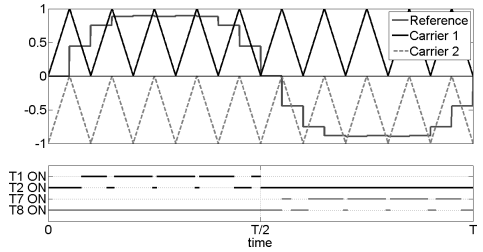

Figure 2. The basic principle of PDPWM technique.

therefore 64 switching combination are allowed. The voltage balancing is not necessary and the load can be balanced among transistors with appropriate control method.

Pulse Width Modulation Strategies Description

Phase Disposition PWM (PDPWM)

PDPWM is a modulation technique utilizing level shifted carriers. The number of carriers depends on the number of converter levels. The PDPWM for the dual converter needs two triangular carriers and one reference signal. The third harmonic can be added to the reference signal to increase maximum voltage in the linear modulation area. As shown in Fig. 2, the upper carrier assumes values from 0 up to 1 and the lower one in the interval from -1 up to 0. Both carriers have the same phase shift. The transistors are switched as follows: In phase a, the transistors of the left converter T1 and T2 are allowed to be switched when the reference signal is in the interval of the upper carrier. The transistors of the right converter T7 and T8 can be switched when the reference signal is in interval of the bottom carrier. If the reference signal is higher than upper carrier, transistor T1 is turned on, otherwise the T2 is turned on and T1 is turned off. If the reference signal is higher than bottom carrier, transistor T8 is turned on, otherwise T7 is turned on.

Carrier Redistribution PWM (CRPWM)

The basic principle of a CRPWM for phase a is shown in Fig. 3. The CRPWM is based on the PDPWM, however in CRPWM, the carriers are composed of two different signals. The first is a zero constant and second is a triangular waveform with variable bias. The bias is changed according to the reference signal. If the reference signal is positive, than the bias is 0, otherwise the bias is -1. To balance the losses of IGBTs, the signals of the carriers are changed once per each period of the reference signal. To avoid

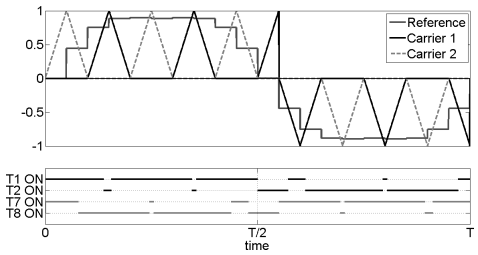

Figure 3. The basic principle of CRPWM.

an increasing in the number of switching, the signal is changed at zero of triangular waveform, when the voltages v_{a1g1} and v_{a2g2} are equal.

Comparison of PWM Strategies

To compare the standard PDPWM and the proposed CRPWM methods the three criteria have been selected as: the total harmonic distortion of the phase load voltage, power losses of the converter, and their distribution among the transistors.

Total harmonic distortion of phase load voltage

For the comparison of the output voltage quality the simulation were carried out with parameters: RL load with resistance $R_L = 1\Omega$, phase load inductance $L_L = 1mH$, dc supply voltage $V_{dc1} = V_{dc2} = 375V$, output frequency $f_{out} = 50Hz$, carrier frequency $f_{PWM} = 1kHz$ and modulation depth $m = 0.9$. The simulated phase load voltage v_{La} and current i_a waveforms of both modulation strategies are shown in Fig. 4 and 5 respectively. The experimentally measured transistor control signals and line to line voltage are shown in Fig. 6 and 7 respectively. The transistor control signals corresponds with the phase to ground voltages v_{a1g1}, v_{a2g2}, v_{b1g1}, v_{b2g2}. The phase to ground voltages are used to obtain line to line v_{ab} are shown in Fig. The line to line voltage is given by formula:

$$v_{ab} = v_{a1g1} - v_{a2g2} - v_{b1g1} + v_{b2g2} \tag{1}$$

It can be seen from those figures that both PDPWM and CRPWM techniques have different phase to ground voltage waveforms. However, line to line, phase load voltage and current waveforms are equal. To quantify the output voltage quality a calculation of voltage total harmonic distortion THD_u has been performed. The formula that describes THD_u is as follows:

$$THD_u = \frac{\sqrt{\sum_{i=2}^{40} V_L^2\,(i)}}{V_L\,(1)}, \tag{2}$$

where i is number of harmonics and V_L represents the phase load voltage.

The result of calculation shown in tab. I indicates that quality of spectral of output voltage in converter controlled CRPWM is nearly equal.

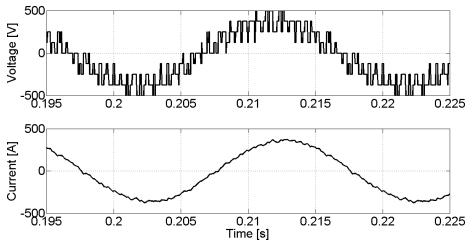

Figure 4. Simulated phase load voltage and current of PDPWM.

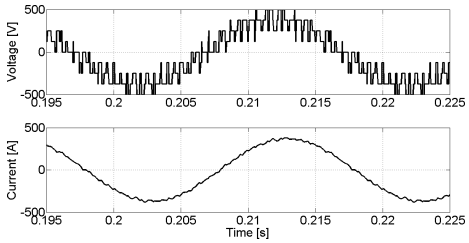

Figure 5. Simulated phase load voltage and current of CRPWM.

Power losses

A series of simulations was carried out to determine dependency of IGBT power losses on a modulation depth and on a power factor. To determine the dependency on the modulation depth, the parameters of simulation were set to $R_L = 0.2\Omega$, $L_L = 0.2mH$, $V_{dc} = 750V$, $f_{PWM} = 1kHz$, $f_{out} = 50Hz$, constant junction temperature $40°C$ and IGBT module No. FZ750R65KE3T produced by the Infineon company was selected. For determination of the dependency on the power factor the impedance of the load was selected as 0.21Ω and R_L, L_L were changed to match different values of power factors.

The total average losses for modulation depth of 0.9 are shown in tab. I. The total power losses of both modulations are nearly equal. Moreover, as can be seen in Fig. 10, depending on modulation depth, the power losses of both modulation are rising with increasing

Table I
THDU AND POWER LOSSES COMPARISON

Modulation strategy	THDu [%]	Average power losses [W]
PDPWM	19.91	45.21
CRPWM	19.86	45.33

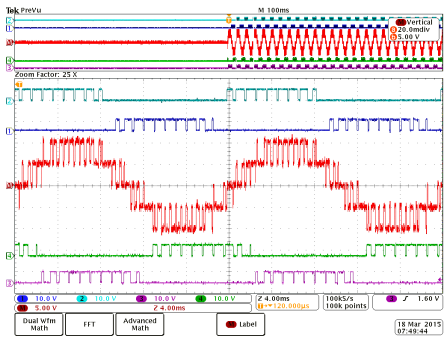

Figure 6. Measured waveform of line to line voltage, (red) and phase to ground voltage v_{a1g1}(cyan), v_{a2g2} (blue), v_{b1g1} (green), v_{b2g2}(magenta) of PDPWM.

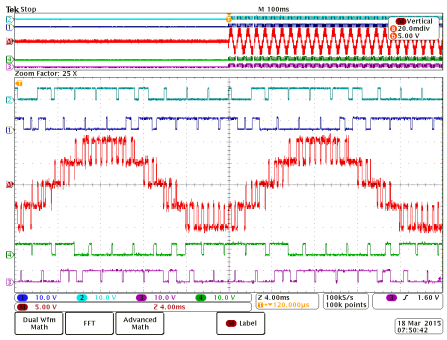

Figure 7. Measured waveform of line to line voltage, (red) and phase to ground voltage v_{a1g1}(cyan), v_{a2g2} (blue), v_{b1g1} (green), v_{b2g2}(magenta) of CRPWM.

modulation depth and are equal over the full range of modulation depth.

However, it appears from Fig. 8 and 9, that the CRPWM has balanced power losses among all of the transistors and the maximum difference of power losses between two transistors is approximately $30W$. On the contrary in the PDPWM the load of transistors is unbalanced and the difference is approximately $410W$. Therefore, maximum power losses of IGBT in converter controlled by the PDPWM are $3.96kW$ and in the case of control by the CRPWM the losses are $3.79kW$ only. Furthermore, as can be seen in Fig. 10, the difference in maximum transistor power losses depending on modulation depth is the most significant around modulation depth of 0.5. Considering results shown in Fig. 12, the maximum transistor power losses are also dependent on the power factor. In the converter controlled by the CRPWM, the losses decrease with decreasing power factor, however, in the PDPWM, the losses increase with decreasing power factor.

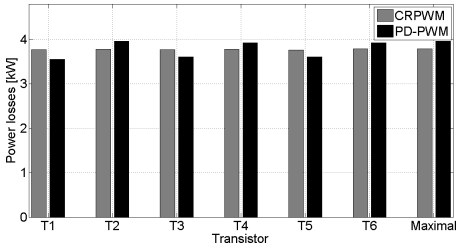

Figure 8. Average power losses of T1-T6 with modulation depth 0.9.

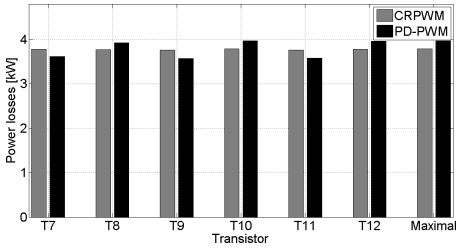

Figure 9. Average power losses of transistor T7-T12 with modulation depth 0.9.

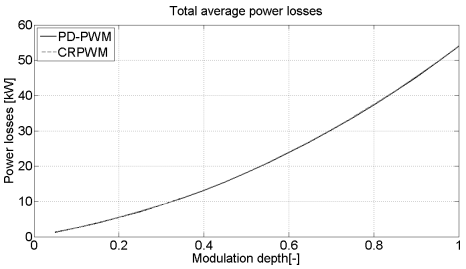

Figure 10. Dependency of Total power losses on modulation depth.

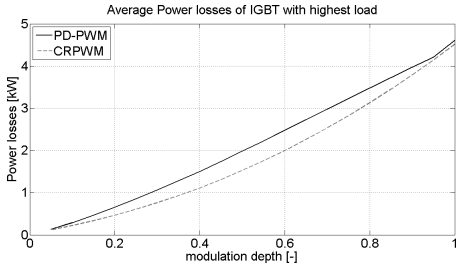

Figure 11. Dependency of power losses of transistor with the highest load on modulation depth.

CONCLUSION

This paper analyzes both the standard PDPWM and a modified PDPWM algorithm for the so called dual inverter composed of two cascaded connected two-level three-phase converters. The modified modulation strategy is widely used as the carrier redistribution PWM (CRPWM) for multilevel converters. This modulation strategy has been adopted for the dual inverter topology in this research and it has been deeply analyzed and compared with a widely used basic phase disposition PWM (PDPWM). The total harmonic distortion of the output voltage obtained by both control strategies are comparable, however, the losses load among the switching devices (IGBTs) in the converter controlled by the proposed CRPWM are lower. Furthermore, in the dual converter controlled by the CRPWM, it is also possible to enhance the output power range. The total losses distribution among the power electronics devices is also better for smaller power factors and also for middle modulation depths. The described theoretical assumptions have been verified by simulations as well as by basic measurement on a real time system with DSP TMS320F28335.

REFERENCES

[1] N. Mittal, B. Singh, S. Singh, R. Dixit, and D. Kumar, "Multilevel inverters: A literature survey on topologies and control strategies," in *Power, Control and Embedded Systems (ICPCES), 2012 2nd International Conference on*. IEEE, 2012, pp. 1–11.

[2] F. Peng, J. McKeever, and D. Adams, "Cascade multilevel inverters for utility applications," in *Industrial Electronics, Control and Instrumentation, 1997. IECON 97. 23rd International Conference on*, vol. 2. IEEE, 1997, pp. 437–442.

[3] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, vol. 3. IEEE, 2003, pp. 6–pp.

[4] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *Industrial Electronics, IEEE Transactions on*, vol. 49, no. 4, pp. 724–738, 2002.

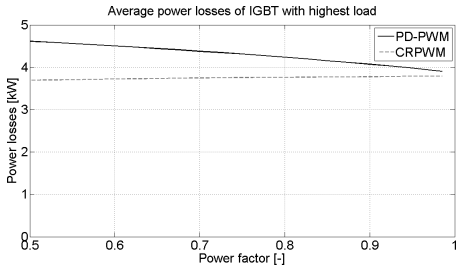

Figure 12. Dependency of power losses of transistor with the highest load on power factor.

[5] M. Khazraei, H. Sepahvand, K. Corzine, and M. Ferdowsi, "A generalized capacitor voltage balancing scheme for flying capacitor multilevel converters," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*. IEEE, 2010, pp. 58–62.

[6] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *Industry Applications, IEEE Transactions on*, vol. 32, no. 3, pp. 509–517, 1996.

[7] K. Corzine, S. Sudhoff, and C. Whitcomb, "Performance characteristics of a cascaded two-level converter," *Energy Conversion, IEEE Transactions on*, vol. 14, no. 3, pp. 433–439, 1999.

[8] B. P. McGrath and D. G. Holmes, "Multicarrier pwm strategies for multilevel inverters," *Industrial Electronics, IEEE Transactions on*, vol. 49, no. 4, pp. 858–867, 2002.

[9] A. Lega, "Multilevel converters: dual two-level inverter scheme," 2007.

[10] M. Sleiman, A. Al Hage Ali, H. F. Blanchette, K. Al-Haddad, B. Piepenbreier, and H. Kanaan, "A survey on modeling, control, and dc-fault protection of modular multilevel converters for hvdc systems," in *Industrial Electronics (ISIE), 2014 IEEE 23rd International Symposium on*. IEEE, 2014, pp. 2149–2154.

[11] D. Krug, S. Bernet, and S. Dieckerhoff, "Comparison of state-of-the-art voltage source converter topologies for medium voltage applications," in *Industry Applications Conference, 2003. 38th IAS Annual Meeting. Conference Record of the*, vol. 1. IEEE, 2003, pp. 168–175.

[12] P. Inttpat, P. Paisuwanna, and S. Khomfoi, "Capacitor lifetime monitoring for multilevel modular capacitor clamped dc to dc converter," in *Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), 2011 8th International Conference on*. IEEE, 2011, pp. 719–722.

[13] J. Mei, K. Shen, B. Xiao, L. M. Tolbert, and J. Zheng, "A new selective loop bias mapping phase disposition pwm with dynamic voltage balance capability for modular multilevel converter," *Industrial Electronics, IEEE Transactions on*, vol. 61, no. 2, pp. 798–807, 2014.

[14] D.-W. Kang, B.-K. Lee, J.-H. Jeon, T.-J. Kim, and D.-S. Hyun, "A symmetric carrier technique of crpwm for voltage balance method of flying-capacitor multilevel inverter," *Industrial Electronics, IEEE Transactions on*, vol. 52, no. 3, pp. 879–888, 2005.

[15] A. Bendre, G. Venkataramanan, D. Rosene, and V. Srinivasan, "Modeling and design of a neutral-point voltage regulator for a three-level diode-clamped inverter using multiple-carrier modulation," *Industrial Electronics, IEEE Transactions on*, vol. 53, no. 3, pp. 718–726, 2006.