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Comparison of Waffle and standard gate pattern base on specific on-resistance

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Abstract:
The main goal of this work is to compare the different Waffle MOS structures as function between main dimensions and channel resistance (specific on-resistance). Even if Waffle MOS structure is so general that it is independent on dedicated CMOS process in fact constrains coming from specific CMOS process design rules has main influence on final Waffle MOS shape and final required area. Comparison describing how dimensions of Waffle MOS have influence on channel resistance would be proposed. Due to non-conventional gate geometry of the Waffle MOS transistor compare to the fingers structure, the channel *W/L* ratio calculation is not trivial and conformal Schwarz-Christoffel Transformation mapping was used.

INTRODUCTION

Due to new power management applications there is more often needs to use smaller power MOS structures or to decrease power MOS resistance without enlarging it area. All of those needs are usually reached by process tuning what is very costly. Other options are design and layout optimization what is on the other hand mainly time consuming and just partial goal should be reached. Alternative solution compare to previous two is to use different power MOS topology which improves the power MOS resistance without process modification. One example of that type of topology is Waffle MOS.

Let's consider simple DC electrical model of the MOSFET for nonrectangular shape of gate electrode in linear region.

$$I_{\mathrm{D}} = \frac{\mu C_{\mathrm{OX}}}{2} \cdot \left(\frac{W}{L}\right)_{EF} \cdot \left(V_{\mathrm{GS}} - V_{\mathrm{T}}\right) \cdot V_{DS} \qquad (1)$$

Where I_D is drain current, V_{GS} is gate to source voltage and V_T is threshold voltage. The μ is a charge-carrier effective mobility and C_{OX} is a gate oxide capacitance per unit area. The $(W/L)_{EF}$ is effective width to length ratio of nonrectangular channel area. And V_{DS} is voltage between Source terminals to Drain terminals.

As was described earlier [1] resistance of interconnect metallization with contacts and with resistance of diffusion between contact to channel are negligible compare to channel resistance. So in this work resistance of channel area will be considered only. For MOS in linear region with source to drain voltage V_{DS} the resistance is as follows.

$$R_{DSON} = \frac{V_{DS}}{I_{\mathrm{D}}} = \frac{1}{\frac{\mu C_{\mathrm{OX}}}{2} \cdot \left(V_{\mathrm{GS}} - V_{\mathrm{T}}\right)} \cdot \frac{1}{\left(\frac{W}{L}\right)_{EF}} \qquad (2)$$

Related to MOS geometry the process design rules have to be defined. Often λ-based design rules are used. Than the relationship between scale factor λ and the feature sizes are as shown in Table 1.[1]

Table. 1: Designed rules for MOS layout

Minimum Dimension Rules	***Name***	***Size***
Poly Width	d_1	λ
Contact Opening	d_2	λ x λ
Contact-Poly Spacing	d_3	λ
Contact-Contact Spacing	d_4	λ
Poly-Contact-Poly Spacing	$d_5=d_2+2.d_3$	3λ

Another aspect which should be considered in the modern process is support of multiple voltage capability. This process feature is available due to using dual or triple gate oxide and larger channel length and source to drain spacing. In this work general dual gate process with two time longer channel length (than minimum polysilicon width) will be considered (allowing two time higher voltage capability). Reason to do so is to describe how

change of process rules is influencing the Waffle MOS resistance area efficiency.

COMPARISON METHOD

The MOS transistors which are mainly used as the switch are usually compared by "specific on-resistance" [6], [7], [8], [9]. This qualitative parameter is taking into account the transistor resistance in on state and area of this transistor. The specific on-resistance sR_{ON} is calculated as multiplication of on-resistance R_{DSON} and transistor area (*Area*).

$$sR_{ON} = R_{DSON} \cdot Area \tag{3}$$

This quantitative figure of merit is usually used to characterize the performance of a device relative to its alternatives. Another alternative usage of the specific on-resistance sR_{ON} is that it should be used for estimation of required transistor area when exact resistance is required.

From known reference element resistance R_{REF} and its element area A_{REF} and from known requested resistance R_{REQ} it is possible to calculate required area A_{REQ} as follows.

$$A_{REQ} = \frac{sR_{ON-REF}}{R_{REQ}} = \frac{R_{REF} \cdot A_{REF}}{R_{REQ}} \tag{4}$$

After insertion of (2) to equation (4) we obtain following equitation

$$A_{REQ} = \frac{A_{REF}}{\left(\frac{W}{L}\right)_{REF}} \cdot \left(\frac{W}{L}\right)_{REQ} \tag{5}$$

where $(W/L)_{REF}$ is effective width to length ratio of reference cell and $(W/L)_{REQ}$ is width to length ratio of requested cell. The area increment describing improvement between requested area and reference element area is as follows.

$$inc_{REQ,REF} = \frac{A_{REQ} - A_{REF}}{A_{REF}} = \frac{A_{REQ}}{\left(\frac{W}{L}\right)_{REQ}} \cdot \frac{\left(\frac{W}{L}\right)_{REF}}{A_{REF}} - 1 \tag{6}$$

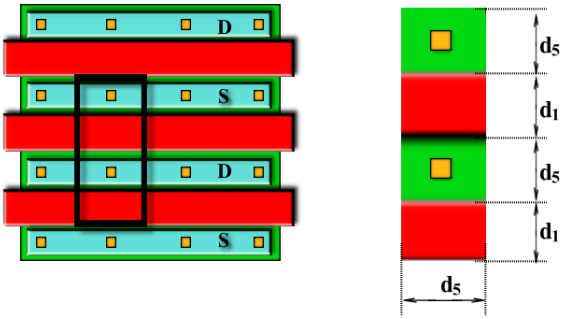
Equation (6) will be used in this work to describe area saving and to compare between two different layouts topologies.

LAYOUT STRUCTURES

Let's consider tree different MOSFET topologies. The first one will be the classical fingers MOS structure, second will be symmetrical Waffle MOS structure with diagonal Source and Drain interconnection, and finely third structure will be Asymmetric Waffle MOS with orthogonal Source and Drain interconnection. First topology will be used as reference to compare other two structures. To allow comparison independent on total area the area of elementary cell will be considered. For each elementary cell area and effective width to length ratio will be defined.

CLASSICAL FINGERS MOS STRUCTURE

One of the most used topology for low voltage MOS is the classical fingers MOS structures with all transistors in one common active area



(a) (b)

Fig. 1: (a) Classical fingers MOS structure (b) Reference element..

The effective width to length ratio $(W/L)_{FING}$ of elementary cell for classical fingers MOS structure is defined as follows

$$\left(\frac{W}{L}\right)_{FING} = 2 \cdot \left(\frac{d_5}{d_1}\right) \tag{7}$$

where d_1 is process parameter describing minimum polysilicon width and d_5 is minimum poly to poly spacing with considering contact between them.

The elementary cell area A_{FING} is defined by minimum distance process parameters as follows

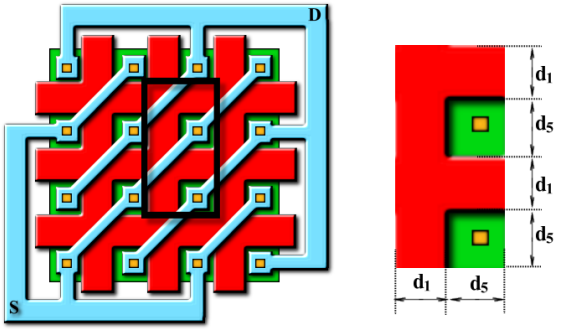
$$A_{FING} = 2 \cdot (d_1 + d_5) \cdot d \tag{8}$$

WAFFLE MOS STRUCTURE

Second topology to be considered is Waffle MOS structure. One of the specifics of Waffle MOS is polysilicon gate (waffle like) pattern and specific stagger Source (S) and Drain (D) terminal arrangement. To reconnect all Source and Drain

staggered terminals usually diagonal metal interconnection routed at 45 degree angle is required.

The sub-element *B* of Waffle MOS (Fig. 4b) has effective width to length ratio with highly nonhomogeneous current distribution. As it was described in previous publication [3] the value of this nonhomogeneous sub-element is not trivial and conformal Schwarz-Christoffel Transformation mapping for calculation was used. Result of the calculation is as follows.



(a) (b)

Fig. 2: (a) Waffle MOS structure (b) Reference element..

The one way how to perform effective channel *W/L* ratio calculation is to constructing a conformal mapping onto a new domain where the problem is trivial. In our case that new domain should be a rectangle [4]. Base on Riemann mapping theorem we know that for any polygon exist mapping to open unit disk. The mapping from unit disk to any polygon is called Schwarz-Christoffel transformations [5]. The mapping *h* from W_1 plane to W_2 plane should be done as composition of two independent SC mapping as shown in Fig. 9. First is inverse SC mapping f^{-1} from element polygon *E* to the unit disk *P*. And second mapping is SC mapping *g* from unit disk *P* to rectangular polygon *Q* [4]

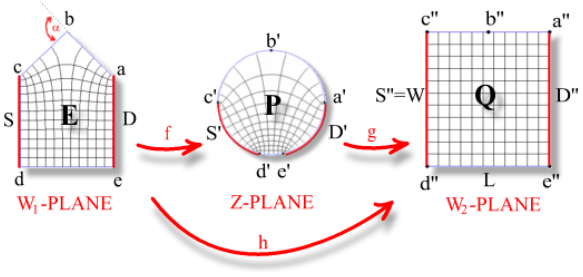


Fig. 3: Conformal map of a elementar polygon onto an equivalent rectangle.

$$f^{-1}(z) = K + C\int_0^z \prod_{k=1}^{5} (1 - w/z_k)^{-\beta_k}\, dw \qquad (9)$$

where *K* , *C* and z_k are unknown complex constants and $|z_k|=1$. The exponents β_k are associated with angles at k-th corners points in plane W_1 and

$$\beta_k = 1 - \frac{\alpha_k}{\pi} \qquad (10)$$

where α_k are exterior angels for points $z_k = \{a, b, c, d, e\}$ in plane W_1 and where $\beta_1 = \beta_3 = 3/4$, $\beta_2 = \beta_4 = \beta_5 = 1/2$.

The mapping *g* from unit disk *P* to rectangular polygon *Q* is

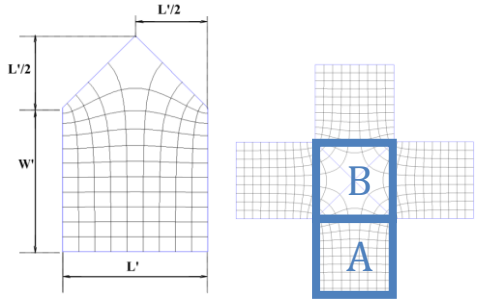
$$g(z) = \int_0^z [t(w)]^{-1/2}\, dw \qquad (11)$$

$$t(w) = (w - a')(w - c')(w - d')(w - e') \qquad (12)$$

The constant *K*, *C* in equation (11) was skipped there because they have only influence on position and scale of the polygon and *W/L* ratio is invariant for them. Because *W/L* ratio of polygon *E* is equivalent to polygon *Q* to get effective *W/L* ratio of *E* it is need to calculate just three points of polygon *Q*

$$\left(\frac{W}{L}\right)_E = \frac{|g(e') - g(a')|}{|g(c') - g(a')|} = 1.1396783. \qquad (13)$$

After composition of four elements *E* we should get macro-element as shown in Fig. 4b. This macro-element contains four times area *A* type on the periphery and one area *B* type located in the center.



(a) (b)

Fig. 4: (a)Proposed element *E* with defined dimensions and containing conformal mapping mash (b) Macro element with orthogonal mesh after SC transformation with area type A and B.

To have effective *W/L* ratio of element *B* it is needed to have effective ratio for region *A* first. In the Fig. 4 we can see that element *A* is not exactly homogenous and contain some small no homogeneity close to the common boundary with element *B* type. To do not lose the high precision of *W/L* ratio reached for element *E*, all no homogeneity of region *A* will be shifted and calculated in already nonhomogeneous element *B* type. It means that we will consider element *A* type as fully homogenous. In our case where width dimension *W'* is equal to length dimension *L'* effective ratio is

$$\left(\frac{W}{L}\right)_A = \frac{W'}{L'} = \frac{|a-e|}{|e-d|} = \frac{L'}{L'} = 1. \qquad (14)$$

The effective *W/L* ratio of element *B* is done as composition of *W/L* ratio of four elements *E* and subtraction of *W/L* ratio of four elements *A*

$$\left(\frac{W}{L}\right)_B = 4 \cdot \left(\left(\frac{W}{L}\right)_E - \left(\frac{W}{L}\right)_A\right). \qquad (15)$$

$$\left(\frac{W}{L}\right)_B = 0.55871 \pm 10^{-5}. \qquad (16)$$

The effective width to length ratio $(W/L)_{WAFF}$ for Waffle MOS elementary cell is defined as follows.

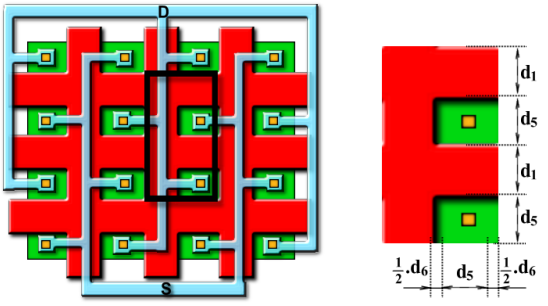
$$\left(\frac{W}{L}\right)_{WAFF} = 4 \cdot \left(\frac{d_5}{d_1}\right) + 2 \cdot \left(\frac{W}{L}\right)_B \qquad (17)$$

The area occupied by Waffle MOS element is defined base on minimum process dimensions

$$A_{WAFF} = 2 \cdot (d_1 + d_5)^2 \qquad (18)$$

ASYMMETRIC WAFFLE MOS STRUCTURE

One disadvantage of Waffle MOS structure is that due to diagonal metal interconnection routed at 45 degree angle in same processes we should violate design rules. In such cases alternative orthogonal routing should be apply [2] (Figure 5). Advantages coming from orthogonal routing are not for free because due to more complex metallic interconnection the larger contact spacing is required and determine.



(a) (b)

Fig. 5: (a) Asymmetric Waffle MOS structure (b) Reference element.

The effective width to length ratio $(W/L)_{A\text{-}WAFF}$ of Asymmetric Waffle MOS elementary cell is defined as follows

$$\left(\frac{W}{L}\right)_{A-WAFF} = 2 \cdot \left(\frac{d_5}{d_1} + \frac{d_5 + d_6}{d_1} + \left(\frac{W}{L}\right)_B\right) \qquad (19)$$

where d_6 dimension represent enlargement of contact to poly spacing compare to minimum dimension due to more complex interconnection. The area occupied by Asymmetric Waffle MOS element is defined as follows

$$A_{A-WAFF} = 2 \cdot (d_1 + d_5) \cdot (d_1 + d_5 + d_6) \qquad (20)$$

COMPARISON

As was mention earlier the equation (6) describing increment of area will be used in this work to describe the area saving and to compare between two different Waffle MOS topologies.

Let's define the area increment for Waffle MOS structure $inc_{WAFF,\ FING}$. The reference element area AREF will be represented by element area of classical fingers MOS structure A_{FING}. And required area A_{REQ} will be represented by element area of Waffle MOS structure A_{WAFF}. After insertion of (7), (8), (17), (18) to equation (6) we obtain following equitation

$$inc_{WAFF,FING} = \frac{A_{WAFF} - A_{FING}}{A_{FING}} = \frac{A_{WAFF}}{\left(\frac{W}{L}\right)_{WAFF}} \cdot \frac{\left(\frac{W}{L}\right)_{FING}}{A_{FING}} - 1 = \frac{d_1 - \left(\frac{W}{L}\right)_B \cdot d_1 - d_5}{\left(\frac{W}{L}\right)_B \cdot d_1 + 2 \cdot d_5} \qquad (21)$$

The area increment for Asymmetric Waffle MOS

$$inc_{A-WAFF,FING} = \frac{A_{A-WAFF} - A_{FING}}{A_{FING}} = \frac{A_{A-WAFF}}{\left(\frac{W}{L}\right)_{A-WAFF}} \cdot \frac{\left(\frac{W}{L}\right)_{FING}}{A_{FING}} - 1 = \frac{d_1 - \left(\frac{W}{L}\right)_B \cdot d_1 - d_5}{\left(\frac{W}{L}\right)_B \cdot d_1 + 2 \cdot d_5 + d_6} \qquad (22)$$

structure $inc_{A\text{-}WAFF,\,FING}$ will be calculated similar way by insertion (7), (8), (19), (20) to equation (6).

If we expect that Asymmetric Waffle MOS has dimension d_6 always greater than zero, from (21), (22) we can get

$$\frac{d_1-\left(\frac{W}{L}\right)_B\cdot d_1-d_5}{\left(\frac{W}{L}\right)_B\cdot d_1+2\cdot d_5+d_6}<\frac{d_1-\left(\frac{W}{L}\right)_{\mathbf{B}}\cdot d_1-d_5}{\left(\frac{W}{L}\right)_{\mathbf{B}}\cdot d_1+2\cdot d_5} \tag{23}$$

From (21), (22), (23) we can get relation between area efficiency of Waffle MOS and Asymmetric Waffle MOS

$$inc_{A-WAFF,FING} < inc_{WAFF,FING} \tag{24}$$

Process parameters to be used for calculation will consider minimum process dimensions. Just for Dual oxide process the two times longer channel length d1 is considered as it is shown in Table 2.

Table. 2: Designed rules for different processes

	Standard process	***Dual Oxide process***
d_1	λ	2λ
d_5	3λ	3λ
d_6	λ	-

Because in Dual oxide process the channel length d1 is considered two times larger, this space is large enough also for more complex orthogonal metal routing of Asymmetric Waffle MOS. Due to this there is no need to reserved additional space for Asymmetric Waffle MOS and d_6 is equal to zero. So Waffle MOS with orthogonal metal routing shouldn't be asymmetrical in Dual oxide process.

The final results comparing different Waffle MOS topologies and different dimensions by using Table 2 and equations (21), (22) are present in Table 3.

Table. 3: : Comparison of Area increment for Different layout structures

	Standard process	***Dual Oxide process***
Waffle MOS	–39.01%	–29.75%
Asymmetric Waffle MOS	–33.85%	-

As it is described in Table 3 the area improvement of Waffle MOS compare to Classical fingers MOS structure is -39.01%. This value is slightly more precise than value -38.9% described by Saqib [1]. Improvement was reach due to using more precise coefficient of element B= 0.55871 instead of 0.55.

WAFFEL MOS LIMIT

As was mention previously change of geometry has significant influence on resistance per area. Due to this we can investigate maximum allowed Waffle gate geometry where MOS topology became ineffective compare to standard finger gate pattern. To find this threshold shape we have to simplify equation (21). To do so let's define aspect ratio (*AR*) parameter as follows.

$$AR=\frac{d_1}{d_5} \tag{25}$$

Where d_1 is polysilicon width and d_5 is minimum polysislicon to polysilicon spacing with contact in the middle. After insertion of equation (25) into equation (21) we can get more simple description of area increment of Waffle MOS.

$$inc_{WAFF,FING}=-1+\frac{1+AR}{2+AR\cdot\left(\frac{W}{L}\right)_B} \tag{26}$$

As it is visible, the area increment of Waffle MOS patter is now dependent only on one variable parameter *AR*. Because of this we can visualize area increment of Waffle MOS in 2D graph (fig. 6).

On the graph it is possible to see not just Standard process area increment and Dual Oxide process area increment but also point where area increment of Waffle MOS become zero. After that threshold point the area increment of Waffle MOS is positive and Waffle gate pattern become no more useful for area saving.

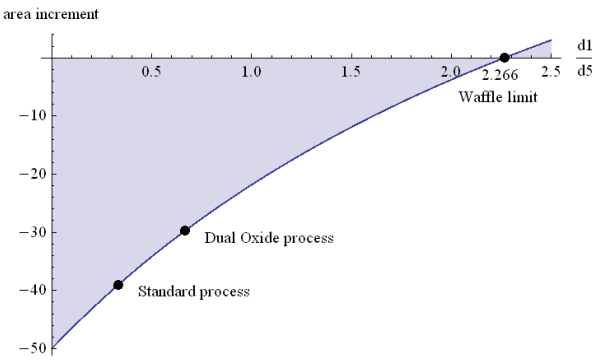


Fig. 6: Area increment dependence on geometry (d_1/d_5) of Waffle MOS structure.

To quantify the boundary of Waffle MOS use case we have to set equation (26) equal to zero. It corresponds to point where area increment of Waffle MOS becomes zero.

$$inc_{A-WAFF,FING} = 0 \quad (27)$$

Under that condition we get from equation (27) specific Aspect Ratio *AR* value as follows:

$$AR = 2.26608 \quad (28)$$

After that ratio (28) the Waffle gate pattern become useless in term of area saving. It means that if polysilicon width d_1 is 2.26608 times larger than spacing between polysilicons d_5, than Waffle gate pattern (compare to standard gate pattern with fingers) is worst in term of resistance per area.

Finally we can define dimensions constrains for Waffle gate pattern where resistance per area is better than with Standard fingers gate patter only when, d_1 is 2.26608 times smaller than spacing between polysilicons d_5,

$$d_1 < 2.26608 \cdot d5 \quad (29)$$

CONCLUSION

Generally Waffle MOS require -39.01% less area compare to Classical fingers MOS while having same resistance. This calculated value is slightly more precise than value -38.9% described earlier by Saqib [1]. Improvement was reach by using more precise coefficient of element *B*= 0.55871 instead of 0.55. Precise coefficient was calculated by using Schwarz-Christoffel Transformation.

In addition comparison of area improvement between Asymmetric Waffle MOS and Waffle MOS shown that Asymmetric Waffle MOS with enlarged poly to poly spacing (due to orthogonal metal routing) has lower area efficiency. This result is in line with previous Madhyastha publication [2] but is more precise due to cross elements *B* consideration.

In multi oxide process where due to higher voltage capability the gate channel length is enlarged (while poly to poly spacing is fixed) the area efficiency is worst.

If polysilicon width d_1 is 2.26608 times larger than spacing between polysilicons d_5, than Waffle gate pattern in term of resistance per area is always worse than standard gate pattern with fingers.

ACKNOWLEDGMENTS

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