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# Practical Design of a Self-Hosted Bandgap Voltage Reference for Automotive Applications

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**Abstract**:
Practical design of a voltage reference based on the well-known self-biased Brokaw bandgap core with bipolar-junction transistors (BJTs) is presented. The voltage reference has its own start-up circuit and a voltage regulator, which is capable of operation even under fast input supply voltage transients and its voltage regulation also removes an impact of the Early effect of the BJTs. The voltage reference operates with an external supply voltage from 5 V to 40 V in the temperatures from –50 °C to 200 °C; it occupies layout area of 0.011 mm$^2$ if the 0.35 µm I3T50 ON Semiconductor technology is used. Simulation results show reference voltage of (1.20 ± 0.08) V is generated across process, temperature and supply voltage spread, including components mismatch.

## INTRODUCTION

The voltage reference is divided into three blocks:

- Bandgap core.
- Voltage regulator.
- Start-up circuit.

The bandgap core generates the reference voltage and a PTAT (proportional to absolute temperature) voltage; it also provides bias current for other blocks and external circuits.
The voltage regulator generates the internal supply voltage from the external supply voltage, which may vary highly and quickly.
Since the bandgap core is self-biased and also provides biasing current to the voltage regulator, which, in turn, provides the internal supply voltage to it, the start-up circuit is needed to ensure the whole voltage reference reaches only the proper operating point (and avoids an bias-less operating point).
Components of the bandgap core have numbering with the first digit being '1', the voltage regulator has '2' and the start-up circuit has '3'.
The voltage reference is designed in the ON Semiconductor I3T50 technology, that forms low-voltage components in isolated N-doped epitaxial pockets. Maximum voltage between any pair of terminal of a low-voltage component should not exceed 3.6 V. The technology allows separation of bulks of MOSTs (metal-oxide-semiconductor transistors); but this should be avoided for P-MOSTs as it requires placing each one in a separate pocket.

## COMPONENT MODELS

Drain (i.e. drain to source) current $I_D$ of an N-MOST operating in the saturation region is given by:

$$I_D = \frac{\mathrm{KP_n}}{2}\frac{W}{L}(V_{GS} - V_{THn})^2, \qquad (1)$$

where $V_{THn}$ is its threshold voltage, $V_{GS}$ its G-S (gate-source) voltage and $\mathrm{KP_n}$ its transconductance constant; $W/L$ is its aspect ratio, with $W$ being width and $L$ length of its channel. Similar formula applies to a P-MOST in the saturation region:

$$I_D = -\frac{\mathrm{KP_p}}{2}\frac{W}{L}(V_{GS} - V_{THp})^2. \qquad (2)$$

The following model expresses a collector current $I_C$ of a BJT (bipolar junction transistor):

$$I_C = \beta I_S e^{\frac{V_{BE}}{mV_T}}, \qquad (3)$$

with $V_{BE}$, $m$ and $V_T$ being voltage across, emission coefficient and thermal voltage of its B-E (base-emitter) junction; $\beta$ denotes the current gain of the BJT. The model is valid only if the BJT operates in the active forward region.

## BANDGAP CORE

The main purpose of the bandgap core (Fig. 2) is to generate the reference voltage $V_{BG}$ with nominal value of 1.2 V. Moreover, the bandgap core provides a biasing current to other blocks and external circuits (as $I_N$ for sinking and $I_P$ for sourcing).

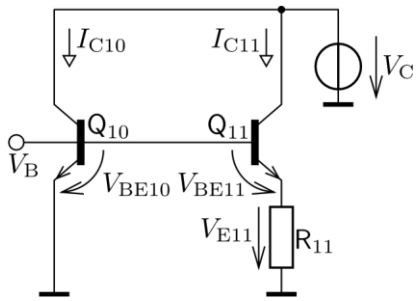


Fig. 1: The non-linear current mirror of the bandgap core

The explanation of the bandgap core shall begin with an analysis of its non-linear current mirror (Fig. 1).

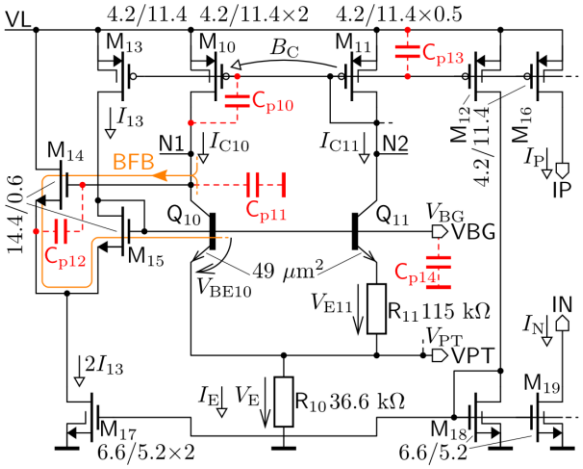

Fig. 2: Schematic of the bandgap core

Let us first assume the collector voltage $V_C$ is high enough to ensure the BJTs operate in the active forward region; the model (3) then gives the collector currents $I_{C10}$ and $I_{C11}$:

$$I_{C10} = \beta A_E I_S e^{\frac{V_{BE10}}{mV_T}}, V_{BE10} = V_B$$
$$I_{C11} = \beta A_E I_S e^{\frac{V_{BE11}}{mV_T}}, V_{BE11} = V_B - V_{E11} \quad . \qquad (4)$$

The rate of growth of the current $I_{C11}$ is less than the one of $I_{C10}$ because of the degeneration caused by the emitter resistor $R_{11}$. An interesting emitter voltage $V_{E11}$ is created if such a base voltage $V_B$ is found for which $I_{C10}$ is $B_C$-times larger than $I_{C11}$ (but not zero) [1]:

$$I_{C10} = B_C I_{C11},\ I_{C10}, I_{C11} \neq 0$$
$$\beta A_E I_S e^{\frac{V_B}{mV_T}} = B_C \cdot \beta A_E I_S e^{\frac{V_B - V_{E11}}{mV_T}} \quad . \qquad (5)$$
$$V_{E11} = mV_T \ln B_C$$

(Simplification equals emitter and collector current of a BJT since its current gain $\beta$ is high enough.) The emitter voltage $V_{E11}$ is just a scaled thermal voltage $V_T$, which is PTAT, as its formula shows:

$$V_T = \frac{k\vartheta}{q_0} \quad [\mathrm{V; J \cdot K^{-1}, K, C}], \qquad (6)$$

where $k$ is Boltzmann constant, $q_0$ is elementary charge, and $\vartheta$ represents the absolute temperature. Besides being PTAT, both $V_T$ and $V_{E11}$ are nearly independent of process variation. The B-E voltages $V_{BE10}$ and $V_{BE11}$ also have small dependence on process variation, but their temperature coefficient (about –2 mV·K$^{-1}$) has an opposite sign.

The circuit in Fig. 2 solves the equation (5) and combines the B-E and the emitter voltage to (almost) remove their temperature dependency [1].

The $I_{C10} = B_C I_{C11}$ condition is set by the current mirror $M_{10}$-$M_{11}$ with its mirroring ratio $B_C$ and kept by the negative feedback loop BFB (as marked in Fig. 2). The feedback loop is closed by the voltage follower $M_{14}$-$M_{15}$, copying voltage from the node N1 to the bases of the BJTs. The feedback is negative because transconductance of the BJT $Q_{10}$ dominates as this BJT does not have its own emitter resistor.

Contrary to conventional practice, both BJTs are identical and the essential non-symmetry for generation of a PTAT voltage is achieved by the current mirror $M_{10}$-$M_{11}$; its mirroring ratio $B_C$ is chosen to be 4, a value that can be realized by composing the transistor $M_{10}$ from two parallel and $M_{11}$ from two series units, as shown in Fig. 3 (a current mirror whose input and output is composed from equal number of transistor units has the lowest mismatch given the same area).

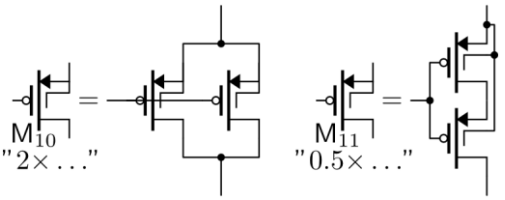

Fig. 3: Parallel and series connection of MOSTs

The emitter voltage $V_{E11}$ varies from 26.6 mV to 56.6 mV across the temperature range (given by (5)). The collector current of the BJT $Q_{11}$ is:

$$I_{C11} \approx I_{E11} = \frac{V_{E11}}{R_{11}}; \qquad (7)$$

the typical resistance of the emitter resistor $R_{E11}$ is set for the current to never exceed 2.5 μA (a trade-off between immunity to leakage currents and current consumption).

Both $R_{10}$ and $R_{11}$ are HIPO (high-ohmic polysilicon) resistors, that have negative temperature coefficient and occupy area of 1.44 μm$^2$ per each 1 kΩ.

Knowledge of the collector current $I_{C11}$ allows designing the aspect ratio of the transistor $M_{11}$ using the following formula:

$$V_L = V_{BG} + V_{THp} + \sqrt{I_{C11} \frac{2}{\mathrm{KP_p}} \frac{W_{11}}{L_{11}}}\ . \qquad (8)$$

A low aspect ratio reduces impact of mismatches of transistors $M_{10}$ and $M_{11}$, but it should not be too low in order for the local supply voltage $V_L$ to not exceed 3.6 V.

The common emitter current $I_E$ can be traced back to the emitter current of the BTJ $Q_{11}$:

$$I_E \approx I_{C10} + I_{C11} = (B_C + 1) I_{C11}. \qquad (9)$$

The common emitter voltage $V_E$ is then a scaled emitter voltage $V_{E11}$:

$$V_E = R_E I_E = V_{E11} D_C (B_C + 1), \qquad (10)$$

The common emitter voltage is available for external circuits on pin VPT as a PTAT voltage. Symbol $D_C$ represents the ratio of the resistances of the resistors:

$$D_C = \frac{R_{10}}{R_{11}}, \qquad (11)$$

(the use of $D_C$ aids in composing the resistors from identical units to improve their matching).

The core idea of a bandgap voltage reference is utilizing a B-E ($V_{BE10}$) and a PTAT ($V_E$) voltages (both of which are almost independent of process variation, and their linear temperature coefficients have opposite signs) and combining them to produce reference voltage $V_{BG}$ that has a very low temperature dependence:

$$V_{BG} = V_E + V_{BE10}. \qquad (12)$$

The low temperature dependence is obtained by appropriate choice of the resistance ratio $D_C$:

$$\frac{\partial V_{BG}}{\partial \vartheta} = 0$$
$$D_C = -\frac{\partial V_{BE10}}{\partial \vartheta} \frac{q_0}{mk(B_C + 1)\ln B_C}. \qquad (13)$$

The formula above gives the resistance ratio of 3.35 (if $\partial V_{BE10}/\partial \vartheta$ is –2 mV·K$^{-1}$ and $m$ is 1); manual tuning according to simulation arrives at 3.14.

Both BJT are vertical with an emitter area of 49μm$^2$.

The purpose of the voltage follower $M_{14}$-$M_{15}$ is to close the feedback loop BFB without loading the node N1 with base currents of the BJTs. Simple source follower is not sufficient, because the node N1 would settle to a higher voltage, requiring the local supply voltage ($V_L$) to be also higher.

The operation of the voltage follower can be explained by the transistor $M_{14}$ being the actual voltage follower, but with its G-S voltage drop being compensated by the transistor $M_{15}$ (precise compensation, although not crucial, requires drain currents of both transistors to be equal, as hinted by the currents $I_{13}$ and $2I_{13}$ in Fig. 2).

The unity gain frequency of the BFB feedback loop is set by the dominant pole, which is predominantly formed by transconductance of the BJTs (including the emitter resistor $R_{11}$) and the parasitic capacitances $C_{p10}$, $C_{p11}$, $C_{p12}$. There two major non-dominant poles:

1. Located at the node N2 and formed by a transconductance of the transistor $M_{11}$ and the gate capacitance $C_{p13}$.
2. Located at node VBG and formed by its dynamic conductance and the parasitic capacitance $C_{p14}$.

Existence of the second non-dominant pole requires limiting the load capacitance of the VBG output in order to keep the BFB loop adequately stable.

## VOLTAGE REGULATOR

The voltage regulator processes the external supply voltage $V_{CC}$ into the local supply voltage $V_L$, which must belong to a low-voltage domain, i.e. not exceed 3.6 V. The idea schematic of the voltage regulator is in Fig. 4.

The voltage regulator maintains such local supply voltage for which the voltages at the nodes N2 and VBG of the bandgap core are equal. This implies equality between voltages at the nodes N1 and N2, greatly reducing an impact of the Early effect of the BJTs on the reference voltage .

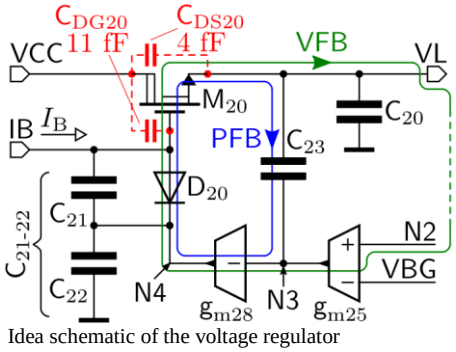

Fig. 4: Idea schematic of the voltage regulator

The pass element of the voltage regulator is the N-DMOST (double-diffused MOST) $M_{20}$ (its D-S voltage can be as high as 40 V, the G-S voltage is limited to 3.6 V).

Operation of the voltage regulator relies on the external biasing current $I_B$, that should be independent of the voltage reference (whose start-up relies on it). Such an independent current source is not part of the voltage reference, because it often requires high-resistance resistor (large in layout area) and it is usually already part of an integrated circuit. The external biasing current may range from 0.2 μA to 60 μA, an interval that is satisfied even by connecting a HIPO resistor of the I3T50 technology between the VCC and IB nodes.

Producing the desired local supply voltage may require a gate voltage of the N-DMOST that is unreachable from a low-voltage domain (i.e. is greater than 3.6 V). Diode $D_{20}$ (Fig. 4) is working as a level-shifter, allowing the gate to be controlled by low-voltage transconductor $G_{28}$; the diode also prevents the transconductor from reducing the local supply voltage below a certain value (important for start-up of the voltage reference).

The voltage regulator should handle large and fast voltage transients on the external supply voltage, as depicted in Fig. 5a. The parasitic capacitances $C_{DG20}$ and $C_{DS20}$ are the reason the transients are penetrating into the local supply voltage; the voltage regulator

compensates them, but not immediately and possibly with an overshoot (Fig. 5b).

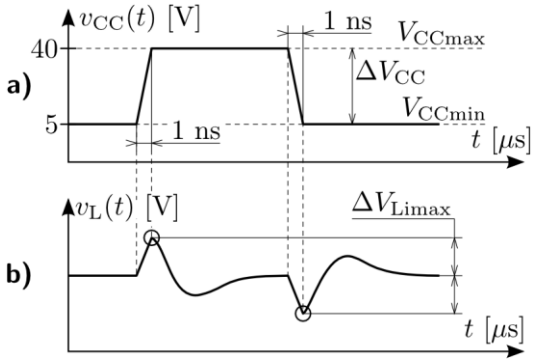


Fig. 5: Voltage transients of the external and local supply voltage

The filtering capacitors $C_{21}$-$C_{22}$ and $C_{20}$ reduce penetration of the voltage transients into the local supply voltage by forming capacitive voltage dividers with the parasitic capacitances $C_{DG20}$ and $C_{DS20}$, respectively. The voltage dividers are most effective if their division ratios are equal; the design formula for the filtering capacitors is:

$$C_{20;\,21\text{–}22} = C_{\mathrm{DS20;DG20}}\left(\frac{\Delta V_{\mathrm{CCmax}}}{\Delta V_{\mathrm{Limax}}} - 1\right), \qquad (14)$$

where $\Delta V_{\mathrm{CCmax}}$ is the maximum step of the external supply voltage and $\Delta V_{\mathrm{Limax}}$ is the designed maximum immediate step of the local supply voltage. Choice of $\Delta V_{\mathrm{Limax}}$ respects $V_{\mathrm{L}}$ to keep $V_{\mathrm{L}}$ in a low-voltage domain (coincidence of a voltage transient with an overshoot caused by a preceding transient should also be considered).

The local supply voltage is maintained by two feedback loops of the voltage regulator: PFB and VFB. The PFB feedback loop reacts to AC disturbances only and provides a dominant pole for VFB (similarly to [2] and [3]), which reacts also to DC disturbances and is responsible for attaining the correct value of the local supply voltage $V_{\mathrm{L}}$.

The open-loop transfer function $F_{\mathrm{PFB}}(s)$ and the unity gain angular frequency $\omega_{\mathrm{U_{PFB}}}$ of the PFB feedback loop is:

$$F_{\mathrm{PFB}}(s) \approx -\frac{g_{\mathrm{m28}}}{sC_{22}}\frac{1}{s\dfrac{C_{20}}{g_{\mathrm{m20}}}+1}, \qquad (15)$$

$$\omega_{\mathrm{U_{PFB}}} \approx \frac{g_{\mathrm{m28}}}{C_{22}},\ p_{\mathrm{nd1}} = -\frac{g_{\mathrm{m20}}}{C_{20}}$$

The dominant pole is located on the node N4; the non-dominant pole $p_{\mathrm{nd1}}$ on the node VL. The RC circuit formed by the filtering capacitor $C_{21}$ with a dynamic resistance of the diode $D_{20}$ can be neglected, because the G-S capacitance of the N-DMOST is much lower than $C_{21}$.

Since one low-voltage capacitor would not withstand the gate voltage of the N-DMOST, the filtering capacitance $C_{21}$-$C_{22}$ is made of two capacitors ($C_{21}$ and $C_{22}$) in series (the diode $D_{20}$ ensures well-defined distribution of the voltage among them).

The open-loop transfer function $F_{\mathrm{VFB}}(s)$ and the unity-gain angular frequency $\omega_{\mathrm{U_{VFB}}}$ of the VFB feedback loop is:

$$F_{\mathrm{VFB}}(s) \approx \frac{g_{\mathrm{m25}}}{sC_{23}}\frac{1}{1+s\dfrac{C_{22}}{g_{\mathrm{m28}}}\left(s\dfrac{C_{20}}{g_{\mathrm{m20}}}+1\right)}. \qquad (16)$$

$$\omega_{\mathrm{U_{VFB}}} \approx \frac{g_{\mathrm{m25}}}{C_{23}}$$

The dominant pole is located on the node N3.

The actual schematic of the voltage regulator is shown in Fig. 6.

The diode $D_{20}$ is implemented as a chain $M_{21}$-$M_{22}$-$M_{23}$, with the bulk not connected to the ground to withstand the gate voltage of the N-DMOST and to reduce the body effect (to make forward voltage of the chain more stable).

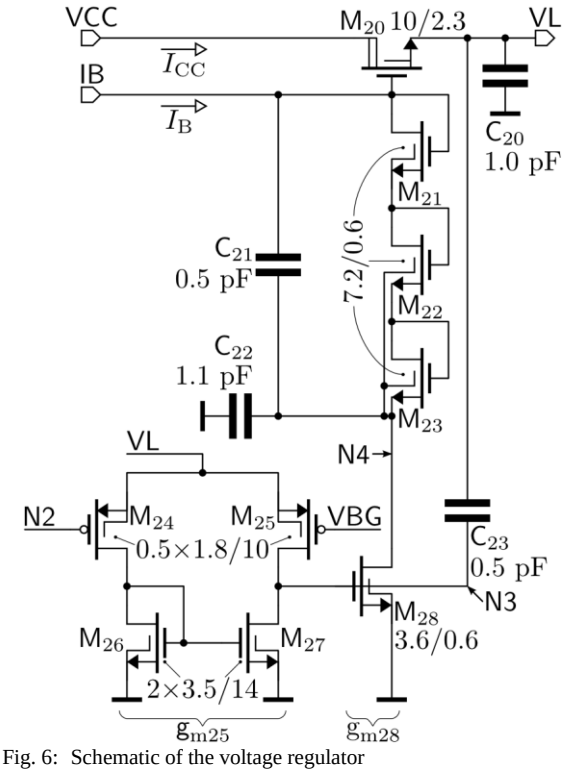


Fig. 6: Schematic of the voltage regulator

All capacitors are low-voltage depletion-mode P-MOSTs, with capacitance density of 4.5 fF·μm$^{-2}$. The capacitance of $C_{22}$ has been increased to obtain good stability of the PFB feedback loop.

The transconductor $g_{m28}$ is a single transistor $M_{28}$; its aspect ratio is a compromise between too high

transconductance (harmful for stability of the PFB feedback loop) and sufficient driving strength to pull down the gate of the N-DMOST as the VFB feedback loop requires.

The transconductor $g_{m25}$ is implemented by a single-stage differential amplifier $M_{24}$-$M_{25}$-$M_{26}$-$M_{27}$. A notable feature of the amplifier is sources of the differential pair being connected to a supply net instead of using current bias. The transistor $M_{24}$ de-facto mirrors a drain current of the transistor $M_{11}$:

$$I_{\mathrm{D24}} = I_{\mathrm{C11}} \frac{W_{24}}{L_{24}} \frac{L_{11}}{W_{11}}; \qquad (17)$$

the drain current of the transistor $M_{25}$ is the same (assuming no mismatch) if the voltages at the nodes N2 and VBG (and therefore N1) are equal. The aspect ratio of the transistors of the differential pair is very low in order to keep the current consumption low; this also results in low transconductance and improved stability of the VFB loop.

The G-S voltage of the transistor $M_{28}$ should not cause $M_{27}$ or $M_{25}$ to operate in the linear region:

$$V_{\mathrm{DSsat27}} \le V_{\mathrm{GS28}} \le V_{\mathrm{D25sat}}, \qquad (18)$$

where $V_{\mathrm{DS27sat}}$ is saturation voltage of the transistor $M_{27}$, and $V_{\mathrm{D25sat}}$ is the maximum drain voltage of the transistor $M_{25}$ for avoiding its linear region:

$$\begin{aligned} V_{\mathrm{D25sat}} &= V_{\mathrm{L}} + V_{\mathrm{THp}} - V_{\mathrm{DSsat25}} = \\ &= (V_{\mathrm{BG}} - V_{\mathrm{THp}} + V_{\mathrm{DSsat11}}) - . \\ -V_{\mathrm{DSsat25}} &= V_{\mathrm{BG}} - V_{\mathrm{THp}} \end{aligned} \qquad (19)$$

## START-UP CIRCUIT

The bandgap core alone has two operating points:

- Started – high enough currents are flowing through the bandgap core, and the voltage reference is fully operational.
- Stopped – there are only leakage currents in the bandgap core.

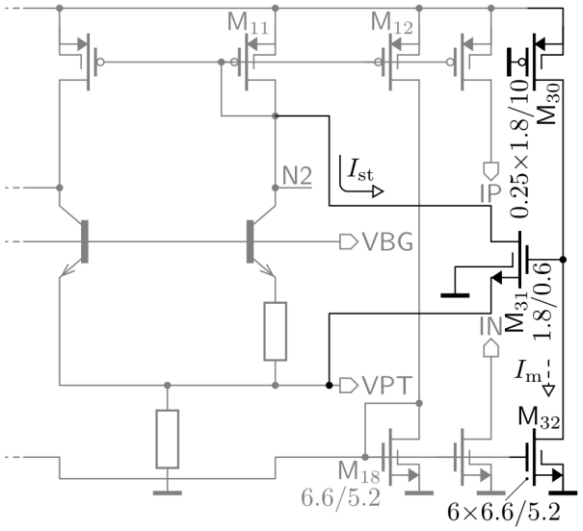


Fig. 7: Schematic of the start-up circuit

The purpose of the start-up circuit (Fig. 7) is to eliminate the stopped operating point.

The current flowing through the bandgap core is mirrored by the transistor $M_{32}$, pulling down the gate of the transistor $M_{31}$, which is also pulled high by the transistor $M_{30}$. If the current is not high enough, $M_{30}$ prevails, opening the transistor $M_{31}$, which starts-up the bandgap core with a start-up current $I_{\mathrm{st}}$.

The transistor $M_{30}$ is a "current reference" (given equal layout area in the I3T50 technology, P-MOSTs provide higher resistance than polysilicon resistors).

The start-up circuit ensures a certain minimum current flows through the bandgap core:

$$\begin{aligned} I_{\mathrm{C11stmin}} &= I_{\mathrm{m}} \frac{W_{11}}{L_{11}} \frac{L_{12}}{W_{12}} \frac{W_{18}}{L_{18}} \frac{L_{32}}{W_{32}}, \\ I_{\mathrm{m}} &\approx \frac{\mathrm{KP}}{2} \frac{W_{30}}{L_{30}} (V_{\mathrm{L}} - V_{\mathrm{TH\,p}})^2 \end{aligned} . \qquad (20)$$

After start-up the transistor $M_{30}$ operates in the saturation region by a small margin.

Non-zero local supply voltage $V_{\mathrm{L}}$ during start-up is ensured by the chain $M_{21}$-$M_{22}$-$M_{23}$ (the voltage regulator might not operate properly at that time).

## SIMULATION RESULTS

The voltage reference has been simulated across corners resulting from combination of parameter values in the table below. "Slow" implies process minimum of threshold voltage and maximum transconductance constant for a (D)MOST, maximum current gain for a BJT, minimum resistance of a resistor, and minimum capacitance of a capacitor ("fast" implies the opposite).

Corners the simulations have been run across

| ***Parameter*** | ***Values*** | ***Simulation*** |
|---|---|---|
| Temperature | –50 °C, 200 C | F, V |
| N-(D)MOST | fast, slow | F, T, V |
| P-MOST | fast, slow | F, T, V |
| Resistor | fast, slow | F, T, V |
| Capacitor | fast, slow | F, V |
| BJT | fast, slow | F, T, V |
| $V_{\mathrm{L}}$ | 5 V, 40 V | F, T |
| $I_{\mathrm{B}}$ | 0.2 μA, 60 μA | F, T, V |

Simulation: F – feedback loop stability ,
T – temperature characteristic, V – voltage transients.

The DC temperature sweep (Fig. 8) shows the reference and the PTAT voltage having low sensitivity to process variations; their strong bending at high temperatures is caused by leakage currents.

The P-type, N-type and supply currents have a non-linear temperature dependency because of originating from a PTAT voltage over a HIPO resistor (which has a negative temperature coefficient).

Mismatch adds a random error of ±37 mV (worst case; 6 standard deviations) to the reference voltage, widening its spread to (1.20 ± 0.08) V.

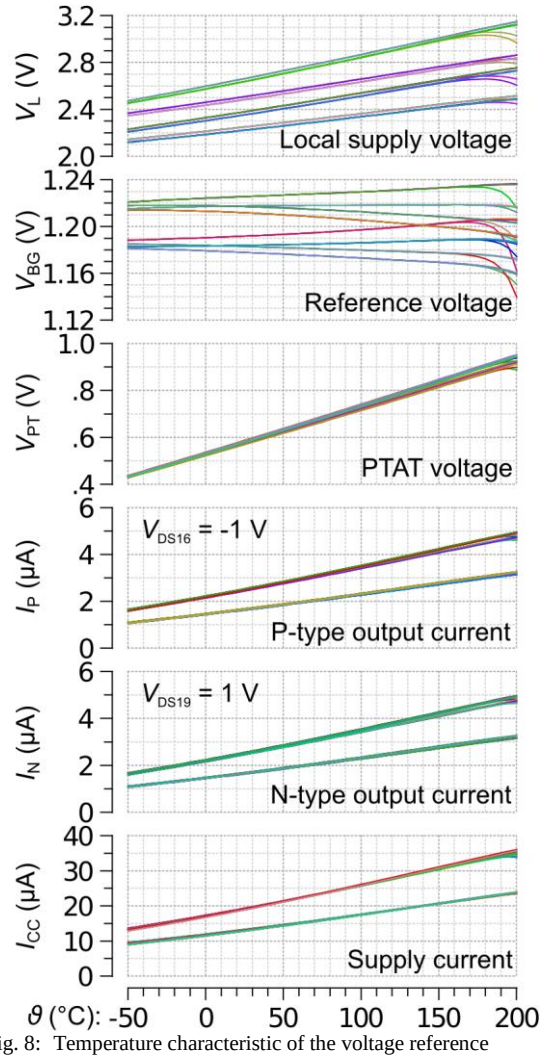


Fig. 8: Temperature characteristic of the voltage reference

The transient simulation (Fig. 9) shows the voltage reference can operate even under fast transients present on the external supply voltage.

Feedback loop stability (small-signal) of the voltage reference

| *Loop* | *Phase margin* | *Gain margin* |
|---|---|---|
| BFB | (53 to 63)° | (–16 to –11) dB |
| PFB | (28 to 103)° | (–78 to –76) dB |
| VFB | (46 to 94)° | (–39 to –17) dB |

The shape of the response of the voltages corresponds to the small-signal stability parameters of the respective feedback loops (listed in the table above).

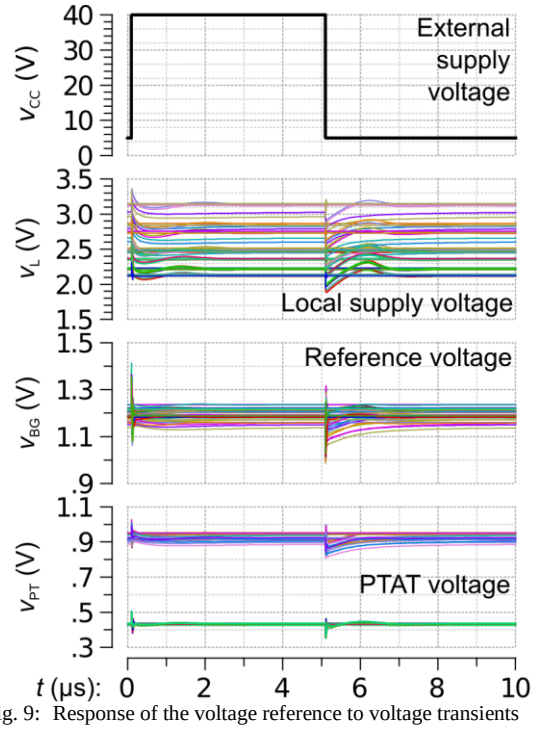


Fig. 9: Response of the voltage reference to voltage transients

## CONCLUSION

The presented reference generates a reference voltage of (1.20 ± 0.08) V, given an external supply voltage from 5 V to 40 V, under process and mismatch variations and the temperatures from –50 °C to 200 °C. Layout area of 0.011 mm$^2$ is occupied if the I3T50 ON Semiconductor technology is used.

The notable feature of the voltage reference is the use of its voltage regulator to set such a local supply voltage for which an impact of the Early effect of the BJTs is removed.

## ACKNOWLEDGEMENT

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